Interfacing Digital Gammasphere with other detectors and systems

This note provides general guidance regarding the types of physical interconnections available between Digital Gammasphere (DGS) and other systems for the purpose of sharing clocks, timestamps and triggers. Discussion of the timing considerations present for different triggering options is provided, with focus upon the methods by which triggers from multiple sources (both internal and external to a given master trigger) and multiple algorithms may be time-aligned for complex coincidence triggers.

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Front panel connections of the DGS master trigger

The master trigger module of Digital Gammasphere provides a variety of different hardware connections, used for a wide set of functions. Figure 1 shows a block diagram of the physical connections of the DGS master trigger.

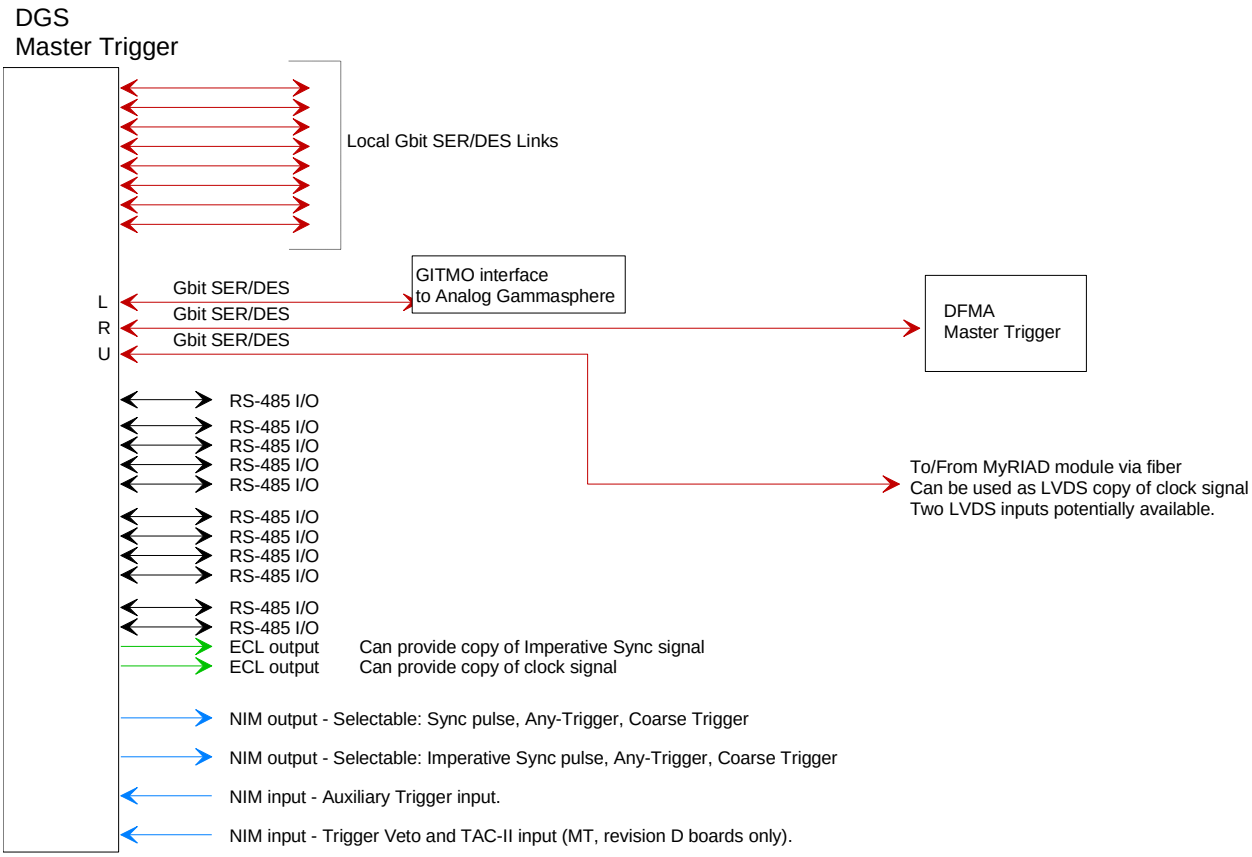


Figure 1 – Block diagram of DGS master trigger I/O connections

The red lines indicate the gigabit/second bi-directional SER/DES links that are used to connect the master trigger to the router trigger and other SER/DES compatible modules such as the LBNL digitizer, the MyRIAD, the GITMO and other master trigger modules. A 13 row by 3 column front panel pin block provides options for connecting single-ended or differential signals. Most of these signals are RS-485, but the bottom two connections are configured as ECL outputs. The master trigger also has two NIM inputs and two NIM outputs with various logical functions defined by firmware.

Anatomy of SER/DES links

Each SER/DES link uses a DS92LV18 chip to send and receive a 1Gbit/second embedded-clock serial data stream. The master trigger has 11 such links, of which 8 (named “A” through “H”) are normally used within the local data acquisition system. The other three links, named “L”, “R” and “U”, are used for interconnects between systems. The overall DGS/DFMA system is shown in Figure 2.

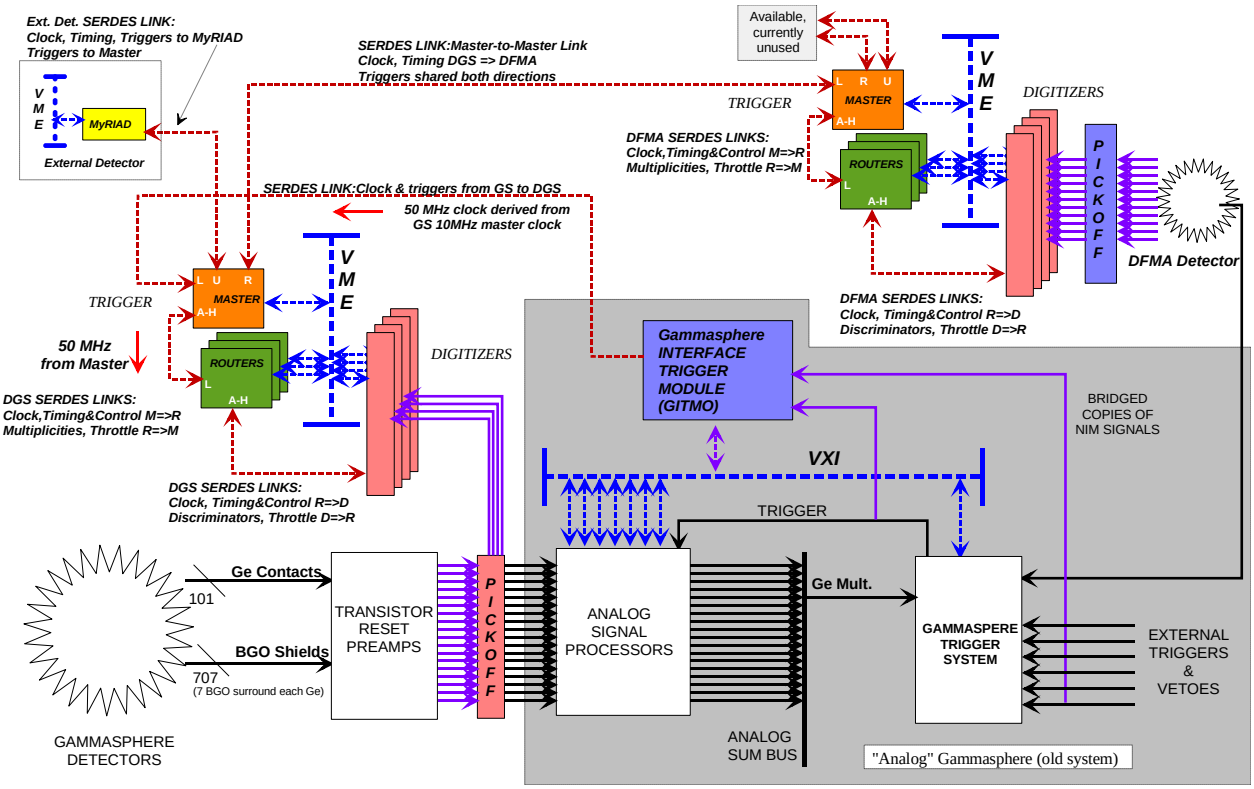


Figure 2 - Complete GS/DGS/DFMA/external multiple-DAQ system.

DGS and DFMA each have their own master trigger, and links “A” through “H” connect the master trigger to link “L” of each trigger router. Links “A” through “H” of the routers connect to the digitzers, forming a hierarchical tree of clock and timing distribution, shown in better detail in Figure 3.

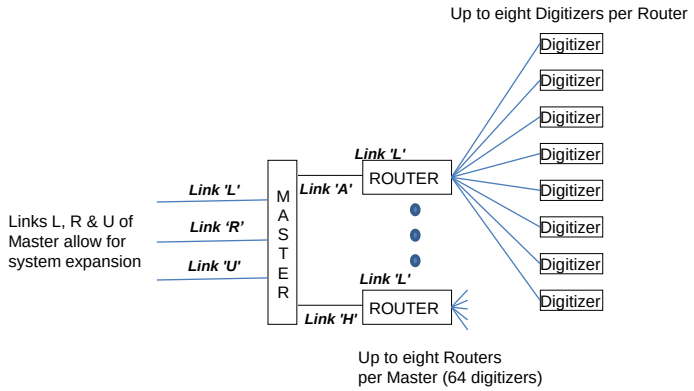


Figure 3 - Detail of master-router-digitizer connections.

At Digital Gammasphere, the “L” link of the DGS master trigger connects to a module named the GITMO (Gammasphere Interface to Trigger Module). The GITMO connects the “analog” Gammasphere data acquisition system to the digital system so that the digital system may use the trigger signals developed by the analog system. The GITMO is not often used now, but was important during the development of the digital system to make comparative performance measurements.

The “R” link of the DGS master trigger is connected to the “L” link of the DFMA master trigger using an optical fiber. Using this link, the two master trigger modules share all clock, timestamp and triggering information with each other. This allows the DFMA system to be synchronized to the DGS system so that both systems run from the same clock & timestamp, plus also allows either system to use triggers from the other.

The “U” link of the DGS master trigger is typically set up as a fiber that runs to a MyRIAD (Multipurpose y-Ray Interface to Auxiliary Detectors) module. The MyRIAD is a 6U VME module intended to be placed into the external detector’s data acquisition system so that local events may be tagged with timestamps sourced from the DGS master trigger. The MyRIAD also can propagate DGS triggers into the external detector and send local triggers from the external detector to the DGS master trigger. Trigger messages from the external detector sent by the MyRIAD may then be coincidence-gated with local Digital Gammasphere triggers to form complex selection criteria for DGS events. The “U” link also contains two LVDS inputs that historically have never been used. These LVDS inputs are available directly to the main FPGA of the master trigger and could, with some firmware development effort, be implemented as general-purpose LVDS inputs to the master trigger.

The data sent from the DGS master trigger is a continuous 1Gbit/sec serial data stream that has a frame structure. One hundred 16-bit words are transmitted every 2 microseconds, broken into 20 frames of five words each. The signal level is LVDS. The data is not DC balanced at the word level and thus the maximum length of copper cable that can be successfully used is 5 meters. The DGS master trigger implements a front-panel fiber optic “paddle card” to send the data stream over longer distances using LC duplex fiber. On the receive side, two different frame-based formats are supported; the DGS master can connect via link “U” to another device sending master trigger format, or the DGS master can work with the simpler MyRIAD data format that consists of a simpler 5-word frame repeated endlessly.

Distribution of the DGS clock to other systems

The master 50MHz clock of DGS can be driven to other systems in a variety of ways.

- If a MyRIAD module is not used with the external system, SER/DES link "U" may be set into a "hardware sync pattern" mode in which the complex serial data stream is replaced by a fixed pattern of 1s and 0s, such that no *data* is transmitted, just the clock. If used in this mode any terminated LVDS signal input of an external detector system can gain access to the clock, but not to the timestamp or any trigger information. The "paddle card" designed for use with the MyRIAD module may be re-purposed to extract this clock from the fiber link.

Figure 4 - MyRIAD fiber adapter paddle card.

- The bottom-most front panel pin connection (AUX I/O B[0]), which is a differential ECL output, may be configured to send the clock of the master trigger to an external device.
- One of the middle front panel pin connections (AUX I/O A[0]) may be configured to be an RS-485 output transmitting the 50MHz clock to an external device. The RS-485 driver is an LTC1689, and 50MHz is near the top of its frequency range, so the quality of this clock output is likely poor in comparison with that available from the other options.

Distribution of the DGS timestamp to other systems

The easiest choice for external systems wishing to gain access to the DGS timestamp is use of the MyRIAD module. If for some reason this option is not available, two methods of obtaining the DGS timestamp remain:

- The user may design a receiver circuit based upon the DS92LV18 receiver chip with appropriate fiber interface, and then implement the necessary state machine logic to recover the timestamp from the serial data stream.
    - Note that the internal SER/DES blocks of modern FPGAs are not compatible with the embedded-clock serialization method used by the DS92LV18, and cannot be used to receive the data stream.
- The user may implement their own timestamp counter that runs from the DGS clock, using one of the methods noted above to receive the DGS clock.
    - When this method is used, synchronization of the local timestamp counter with that of the DGS master trigger is required. The DGS master trigger issues an Imperative Sync command over the SER/DES to tell all the DGS digitizers to reset their timestamp to zero.
    - As shown in Figure 1, this Imperative Sync command can be copied to external systems by configuring either the 2nd ECL output, or one of the two NIM outputs of the master trigger, to send a pulse whenever an Imperative Sync command is issued.

Sending triggers from DGS to external systems

Digital Gammasphere is a buffered timestamp-based system, which means that triggers need be neither prompt nor fixed in delay. In DGS, the firmware architecture of the digitizer boards performs pileup calculations before alerting the trigger of discriminator activity, and thus the trigger is not informed of discriminator firings until microseconds after they occur. Similarly, since selection of events within the digitizers is based only upon the comparison of timestamps with no real-time coincidence required, the trigger is free to have variable delay from when the trigger decision is made to when the trigger decision is broadcast. This allows the trigger to be state-machine based with small FIFO buffers that hold trigger decisions from the moment they are made until the state machine comes back around to the point where trigger decisions are broadcast. In the master trigger, decisions are held in these FIFOs for up to two microseconds. While highly flexible and also powerful, this architectural choice complicates transmission of triggers from DGS to non-buffered external systems.

The MyRIAD module provides logic to address the variability of delay in the trigger message transmission by providing a state machine that repeats the DGS trigger on a NIM output at a fixed delay relative to the gamma-ray discriminator firing. This is accomplished using the timestamp in the trigger message and the internal timestamp of the MyRIAD (which is synchronized to that of the master trigger). Unfortunately, this does not eliminate the overall delay incurred by the buffered system and thus this output often occurs too late for many external, non-buffered detector DAQ systems.

In an effort to provide a fast trigger signal to external detectors, the DGS system implements what is known as the “coarse trigger”. There are two forms of the “coarse trigger” available, the “Any Ge” and the “fast sum”. It is **critically important** to understand that the “coarse trigger” is formed by the DGS system *using the signals before any digital filtering or pileup rejection occurs.* The “coarse trigger” is formed by a distinct and separate discriminator logic block that is optimized for speed rather than accuracy. Because of this, *the “coarse trigger” discriminator may fire on noise or on pileup events that the main discriminator will not.* Thus, the “coarse trigger” can provide “false positives” that cannot be eliminated; such occurrences will generate signals to the external detector that have no corresponding event in DGS and will have to be sorted out by analysis software.

The “Any Ge” coarse trigger

As the name implies, this coarse trigger simply indicates whether any Ge Center detector signal in Gammasphere fired. Each digitizer module internally generates a coarse discriminator signal for each of the five Ge Center signals (channels 5-9), and the logical OR of these signals is sent to the trigger router over a non-serialized dedicated LVDS line. Inside the Routers, a dedicated CPLD chip separate from the main FPGA receives the “any Ge” bit from each of the digitizers connected to the router trigger module, forming the logical OR of all those bits and sending that over a front panel ribbon cable to the master trigger. Within the master trigger, the logical OR of the ORs from the Routers may then be driven out to any of the RS-485 pins, either ECL output or either NIM output. The propagation delay of this coarse trigger is fast (less than 500ns) but no multiplicity information is retained; it is simply the OR of all Ge coarse discriminators.

The "fast sum" coarse trigger

The "fast sum" coarse trigger allows the generation of a fast, coarse multiplicity-based trigger. Similar to the way the "Any Ge" coarse trigger is formed, the CPLDs of the router and master trigger boards are used for speed. However, instead of using a dedicated LVDS line, the digitizer module instead sends the five coarse discriminator bits over the SER/DES link to the router trigger module. The router's main FPGA then internally transmits the partial multiplicity sum to the CPLD chip. The same front panel ribbon cable connection between routers and master trigger is again used, but now to send the partial multiplicity sums from each router to the master trigger. The master trigger CPLD then forms a sum-of-sums, compares that value to a threshold, and issues the trigger if the multiplicity exceeds the threshold.

The formation time for the "fast sum" coarse trigger is still relatively quick (less than 1usec), but due to the mixed use of CPLDs plus some SER/DES communication a small amount of jitter (+/-40ns) is to be expected. As with the "Any Ge" coarse trigger, the "fast sum" trigger may then be driven out to any of the RS-485 pins, either ECL output or either NIM output.

The "Any Ge" and "fast sum" modes are mutually exclusive. One or the other may be set up to come out of the master trigger but both are not available simultaneously.

Receipt of triggers from external systems by DGS

The MyRIAD module is designed to collect local trigger signals (either NIM or ECL), latch the DGS timestamp when the local trigger occurs, and then also send the trigger to the DGS master trigger over the SER/DES interface. The MyRIAD provides two types of "external trigger" to DGS, the "raw" and the "gated". The MyRIAD "raw" trigger is sent immediately upon receipt of the local trigger signal. The "gated" trigger is sent after the "raw" trigger has been confirmed by coincidence (within a programmable timeout) with a second local signal, applied to a different NIM input of the MyRIAD.

The DGS master trigger receives both the "raw" and "gated" MyRIAD triggers, and enters that trigger request into a logic block that provides both timing alignment and additional coincidence gating with internal DGS triggers, as shown in Figure 2. The MyRIAD trigger message may be delayed by a programmable time, in order to align the external detector's trigger with the buffering delays of the DGS digitizer firmware. Additionally, a selection matrix allows an arbitrary selection of internal DGS triggers to be connected to coincidence logic so that only those MyRIAD trigger requests that occur within a programmable time window of an internal DGS trigger condition cause a DGS event selection.

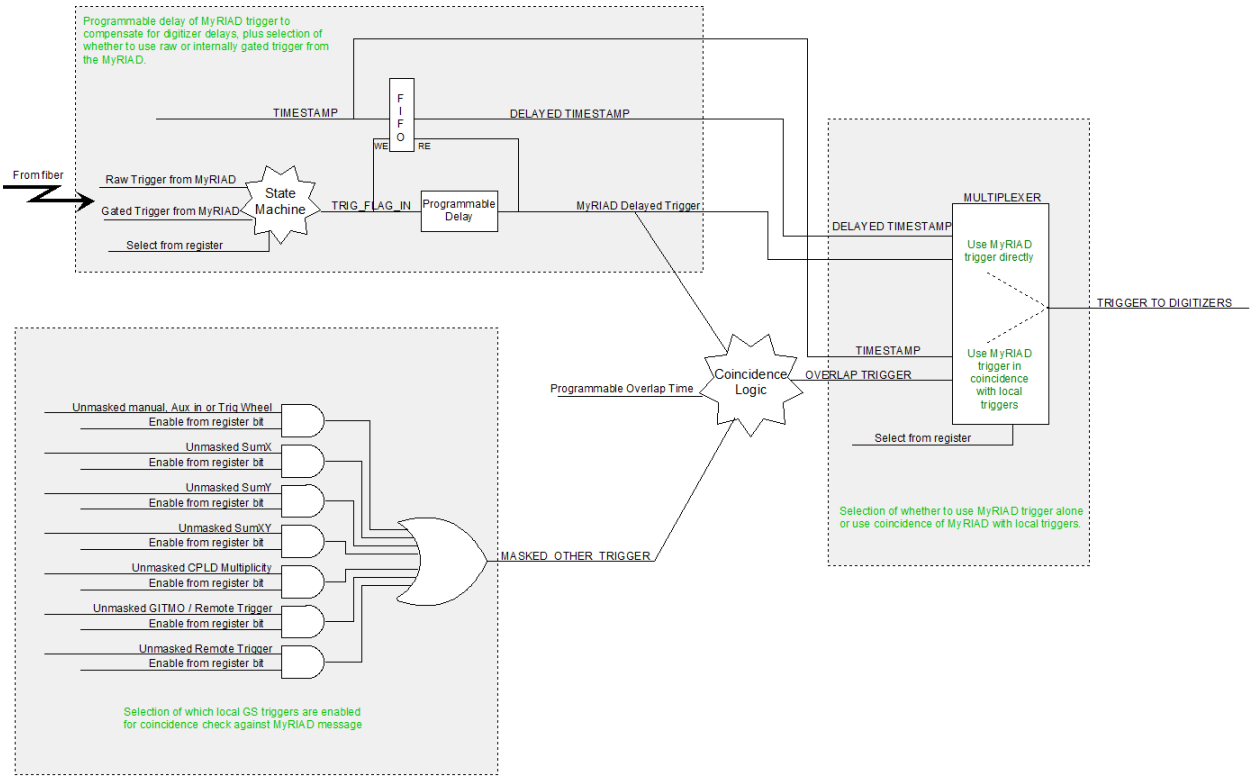


Figure 5 – DGS Master Trigger processing of trigger messages from the MyRIAD

Use of external triggers without a MyRIAD

If the external detector system does not use the MyRIAD, a NIM Auxiliary Trigger signal may be connected from the external detector to the DGS master trigger. In this case, a programmable delay akin to that provided for the MyRIAD trigger is used to compensate for the buffering delay so that the external trigger is properly aligned with the discriminator firing for the same event. Unlike the MyRIAD interface, the Aux Trig In currently does not provide any additional coincidence logic to allow further selectivity.

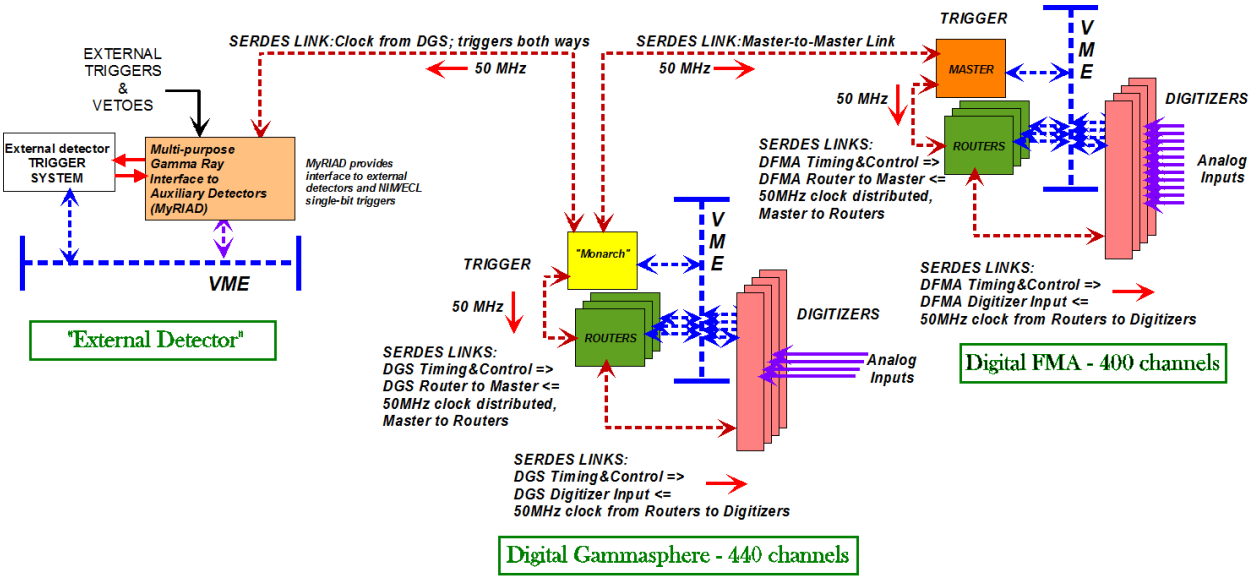
Timestamp alignment of triggers between disparate digital systems

A complex scenario occurs when attempting to combine triggering information from two digitizer-based systems such as DGS and DFMA. In this setup, two master triggers are connected together and one of them is declared the “system monarch”. The “system monarch” is the master trigger who has two distinctions:

1. The “monarch” is the root source of the clock and the Imperative Sync. Another way to define this is that every master trigger that receives timing & control information on link “L”, and thus is capable of using some other master’s clock, is *not* the “monarch”. In the usual setup at Gammasphere, the DGS master trigger is the “monarch” and the DFMA master trigger can be configured to run independently or to use the clock from DGS.

2. By extension, the “monarch” is the master trigger that is nominally expected to receive and re-propagate trigger messages from the other master trigger into the domain of the “monarch”. This isn’t strictly true, as any master trigger can set its **Propagation Control** register to allow or disallow re-propagation of any other master’s local triggers, but as will be discussed in this section the timing relationships across masters make propagation in both directions a potentially overcomplicated setup.

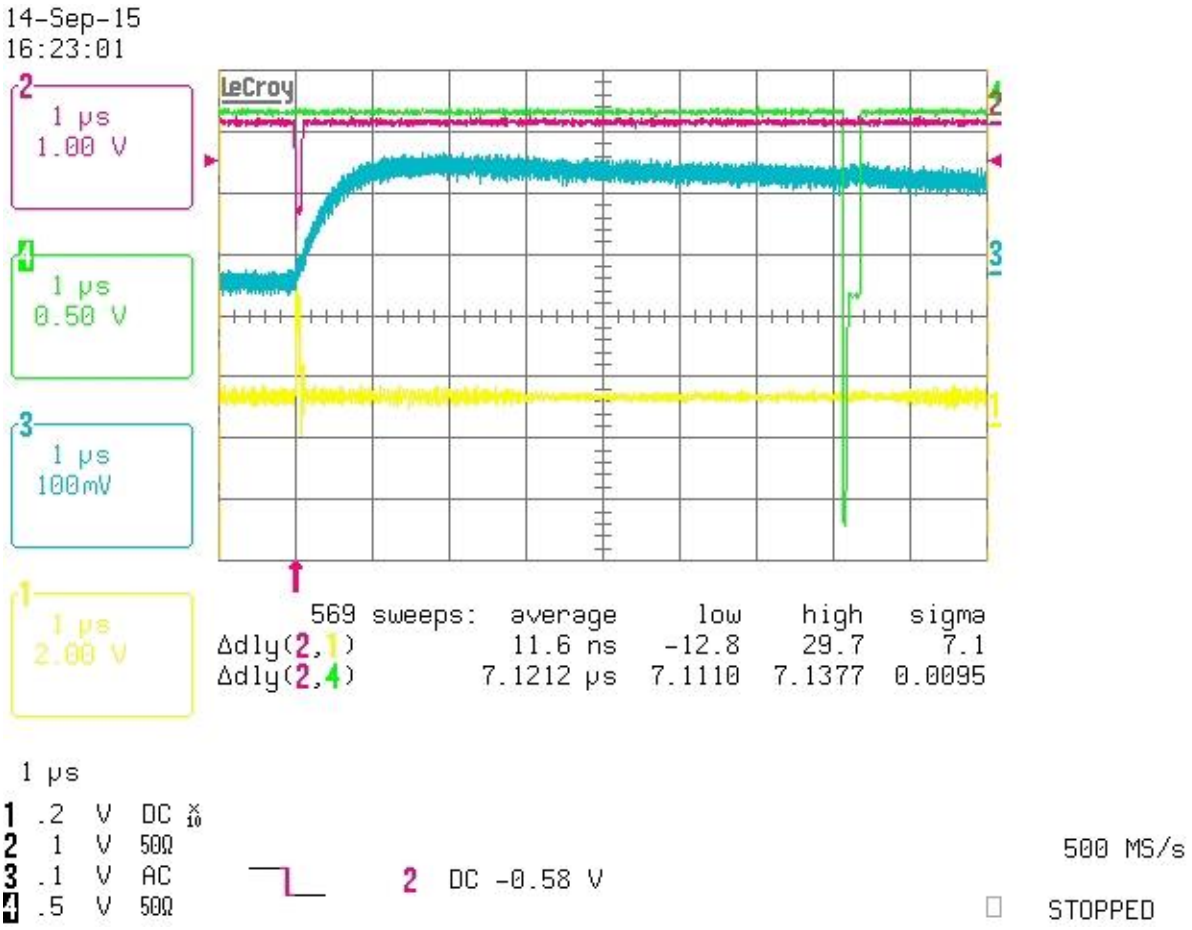
The generic connection being discussed here is as given in Figure x.



The “monarch” (DGS master trigger) provides the clock and timestamp synchronization to both the DFMA master trigger and a MyRIAD module in an external detector. While all clocks and timestamps are fully synchronized, there will be *offsets* between the timestamps in various places.

Timestamp offsets of events *within a system*

Within a given digital system (DGS or DFMA), the digitizer modules are all synchronized to the master trigger. However, at any given moment of time (as given by the clock on the wall), the timestamp in the digitizer will lag behind that of the master trigger due to the propagation delays experienced by the Sync message as that message first goes from master to router, then through the router, then from router to digitizer. This offset has been measured in the test stand, as shown in Figure Y.



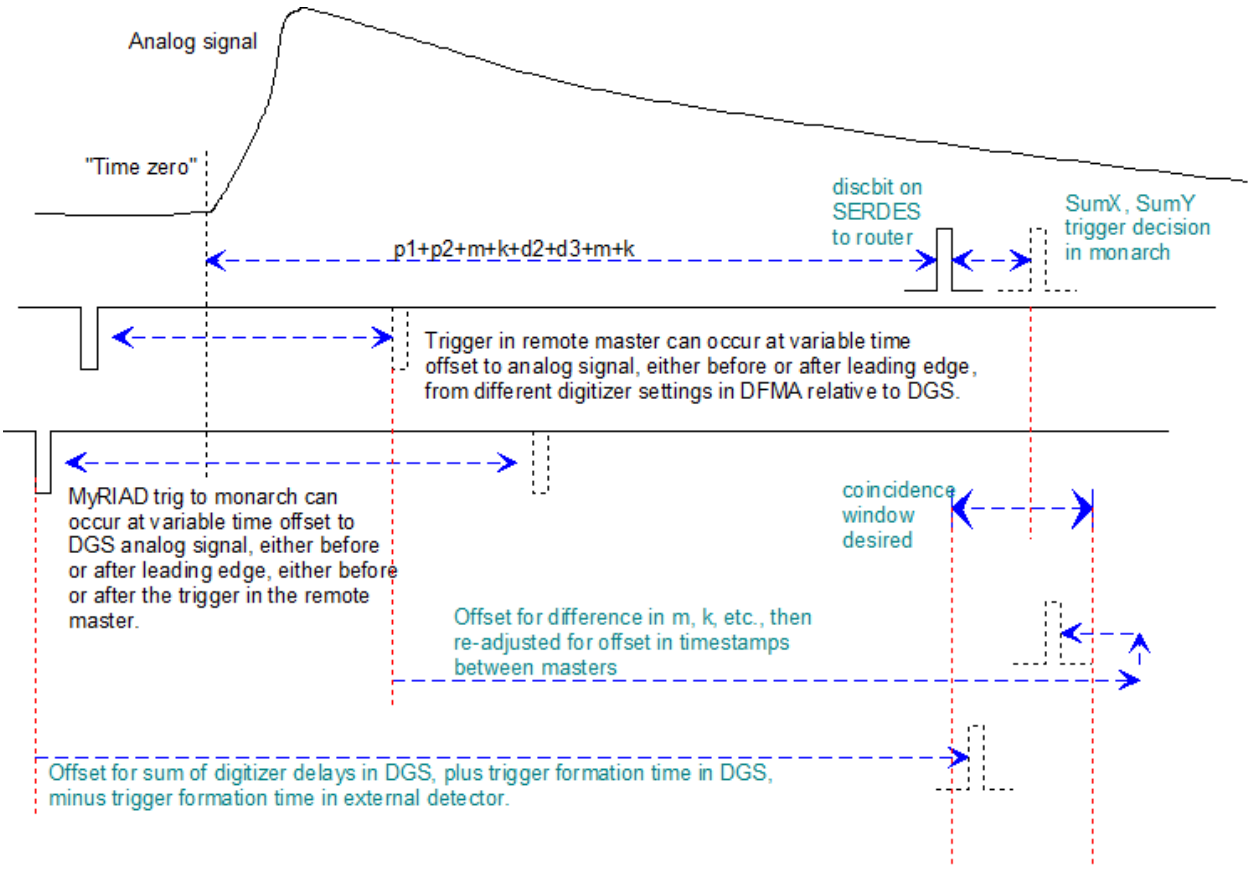
The red trace is a NIM output that is synchronous to the analog signal, whose delay may be adjusted. The analog signal (blue) is a copy of the analog signal as driven out the monitor DAC output of the digitizer. The yellow signal is the coarse (fast) discriminator output of the digitizer. The red trace has been aligned to occur at the same time as the yellow signal. After this is done, the same cable from which the red trace is drawn is connected to the NIM Auxiliary trigger input of the master trigger. The timestamps of the events as marked by the digitizer, and the timestamps of the Auxiliary trigger inputs, are saved. The delayed NIM output of the waveform source may also be visually aligned with the digitizer's DAC output, with the DAC displaying the waveform as it falls out of the 'k' buffer.

This latter setup (where both waveform and red trace are delayed) is a simpler calculation, as it eliminates worrying about what 'p1', 'p2', 'm' and 'k' are set to. In this case the discriminator timestamp latching would be expected to occur 19 clocks (190ns) after the NIM output as the threshold is set low. Examination of the trigger firmware shows that the timestamp latched by the trigger is expected to be offset by 120ns, the number of clock ticks it takes the master trigger to respond to the NIM input. Thus the expected difference between the timestamps should be 190 – 120, or 70ns apart. The timestamps measured are 660ns apart, leaving a residual timestamp offset of 590ns between digitizer and master trigger.

Timestamp offsets *between two digitizing systems*

In similar fashion, in the system of Figure x the timestamps in the MyRIAD and DFMA master trigger modules is expected to run synchronous to but behind the timestamp in the DGS master (the "monarch"). If a particle-gamma interaction were to leave signals simultaneously in the digitizers of DFMA and DGS, the timestamp contained within the trigger message formed by the DFMA master from its local SumX algorithm will have a different timestamp than the one contained within the trigger message formed by the DGS master from its local SumX algorithm. There is an irreducible offset from the master-to-master communication, but this is further complicated by the fact that the 'm', 'k', 'p1', 'p2', 'd' and threshold settings will almost certainly differ between the two setups.

These variations between the systems create havoc for the DGS master (the "monarch") if the experimental desire is to trigger and read out DGS events only when a time-coincidence of triggers between DGS and DFMA occurs. If all digitizer parameters are set the same way in both systems the timestamp value in the DFMA trigger accept messages will always be a smaller number than those of DGS. For perfect matching an offset value would have to be added to the timestamp number in the DFMA messages and the coincidence formed between the local DGS trigger message time and the offset DFMA trigger message time. This is illustrated in Figure x, where the time at which the triggers *actually occur* in the MyRIAD and/or a remote master trigger can vary relative to when the local DGS trigger occurs. Depending upon cabling setups and time-of-flight, a MyRIAD trigger could conceivably even arrive at the DGS master trigger before the analog edge even enters the digitizer ("time zero").



The offset value required for a DFMA (remote master) trigger would have to account for the differences in digitizer parameters between the systems, in addition to the irreducible timestamp offset. As 'm' can vary over a much larger range than the expected timestamp offset between the systems, the offset that would have to be applied to a DFMA number might then have to be a *negative* number once all differences are accounted for. Because of this, the coincidence may not work as desired because the DFMA trigger message would arrive too late for the offset time coincidence to work out. The only way to handle such scenarios is to perform two separately calculated numerical adjustments on the timestamps contained within the trigger accept message from a remote master trigger.

When a local DGS trigger algorithm is satisfied, an internal pulse is generated that is applied to a coincidence logic block. When a remote trigger from the DFMA master is received, the timestamp within that message is numerically adjusted by the two offset considerations. This adjusted timestamp value is compared against the timestamp within the DGS master, and when the local timestamp matches the

On September 15, 2015, two new 16-bit registers, REMOTE_TRIG_TS_OFFSET and REMOTE_TRIG_DIG_OFFSET, were added to the master trigger build. When a remote trigger from another master trigger is received, the timestamp of the trigger message is offset by adding the value in REMOTE_TRIG_TS_OFFSET and *subtracting* the value in REMOTE_TRIG_DIG_OFFSET. This adjusted value is then re-propagated to the digitizers of the local system.

To ensure sanity, a coincidence trigger would hold itself disabled until both TS(DGSfp) and TS(DFMAfp) are both positive numbers. The loss of events during the first 10-20usec of a run is inconsequential. Once all the offsets are applied, the difference between TS(DGSfp) and TS(DFMAfp) may then be compared against window constraints, and a trigger issued if the difference fits within the window. Within DGS, of course, that trigger would be issued with the DGS internal timestamp *at the time the coincidence window calculation is satisfied*, with no offsets. This would provide consistent digitizer event selection window values with a local-only trigger.