Fast CPLD sum logic in router and master

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This note will attempt to give the use model and typical setup for the CPLD sum logic in Digital Gammasphere. Where useful, comparisons to GRETINA usage are provided for reference.

Introduction

In Digital Gammasphere (DGS), the digitizer modules generate a fast discriminator bit referred to as the *coarse* discriminator in the five Ge channels (channels 5-9) in addition to the normal pileup-modulated, filtered discriminator bit provided for all 10 channels. All 15 of these bits are transmitted over the SERDES link between boards. The *coarse* discriminator bit comes out much faster and its timing is not dependent on 'm', 'k' or any of the other usual DGS timing parameters, but the activity of the *coarse* discriminator bit is controlled by the following digitizer parameters:

- While the *time delay* of the coarse discriminator is fixed at 160ns (16 clock ticks), the *coarse* discriminator shares the same discriminator threshold as the main leading-edge discriminator.
    - Optimal performance of the *coarse* discriminator is, therefore, achieved when the 'd' parameter is also set to 16.
- The *coarse* discriminator uses the ADC signal ***after*** the P1 delay, but ***before*** the P2 delay; thus the latency of the *coarse* discriminator will be dependent upon the P1 setting.
    - The P1 delay value ranges from 0 to 15, and is normally set to 1 in all channels.
    - P1 is only adjusted away from 1 if used to compensate for cabling delay differences within DGS.

The *coarse* discriminator bits are sent over the SERDES link to the router trigger boards. A router receives the SERDES bits, the main FPGA of the board calculates the partial multiplicity sum and passes that over to the CPLD of the router board using internal wiring. A separate set of singular LVDS bits (one per digitizer) are also connected. In DGS these singular bits are programmable as various signals from the digitizers. See Figure 1.

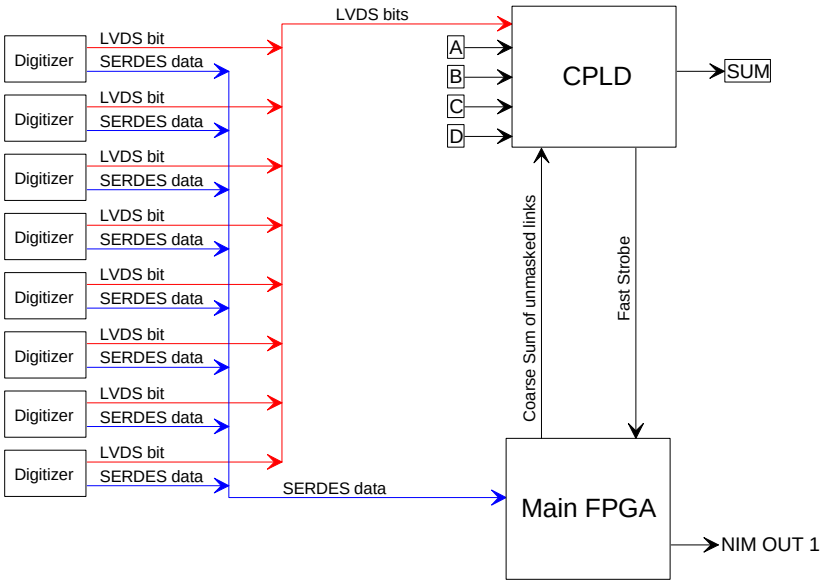

Figure 1 - Connectivity of the CPLD in the trigger module

Comparison to the GRETINA model

In the GRETINA model separate discriminator bits per digitizer channel are not provided to the trigger router through the SERDES link. Instead, only the channel deemed the "central contact" (channel 9) is provided, and this single bit is sent to the trigger router over the separate reserved LVDS pair (in the same cable as the SERDES link, but on different pins). The router receives these singular bits (one per digitizer) using an LVDS transceiver chip and the 8 raw bits are presented directly to the CPLD chip.

CPLD block diagram

The ***same*** CPLD program is used by both the router and master trigger of DGS. To properly understand how this is possible, refer to Figure 2.

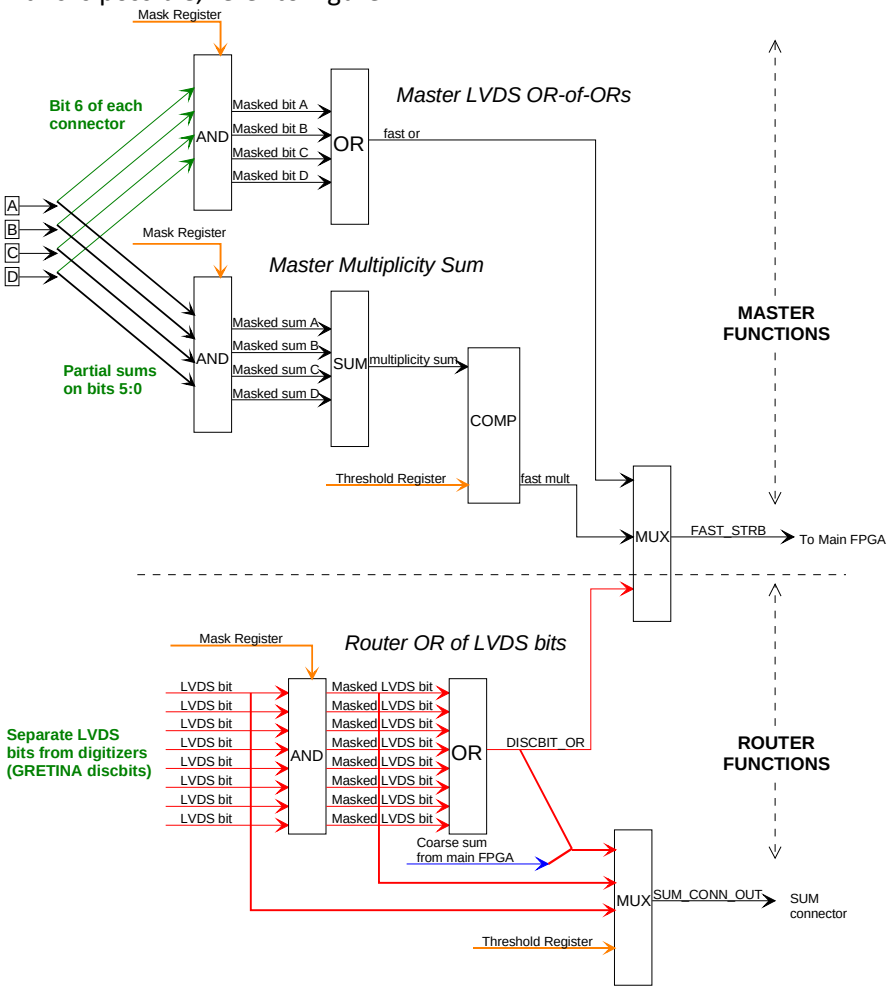

Figure 2 - Block diagram of CPLD

The ***RED*** portion of the CPLD logic is that which is generally active in a router trigger. A DGS router uses the *coarse sum from main FPGA* input, along with the DISCBIT_OR, and sends that to the master trigger. The ***BLACK*** portion (top 2/3rds) is the master part of the logic. The master trigger collects data from the SUM outputs of routers on inputs A,B,C,D and forms both a total multiplicity sum and a collected "OR-of-ORs" from all the LVDS bits of all the digitizers. The multiplicity sum is compared against the threshold register and the user may select between the threshold comparison and the "OR-of-ORs" as the source of the FAST_STRB signal routed to the main FPGA. The main FPGA may then use the FAST_STRB as a source of trigger, a source of a NIM output, or both.

Comparison to the GRETINA model

Use of the DISCBIT_OR on the SUM connector in routers and the "OR-of-ORs" in the master trigger provides a way to form a fast multiplicity>0 signal, but a different version of router CPLD is required in cases where GRETINA would want a multiplicity>n fast trigger as a sum of the masked LVDS bits is required. Separate and distinct GRETINA CPLDs are maintained for this purpose.

Front panel connectivity of the CPLD

The connectors labeled A, B, C & D are input connectors. In a router these have no useful function. In the master trigger, the A, B, C & D inputs are expected to be connected by short ribbon cables to the SUM outputs of up to four routers as shown in Figure 3.

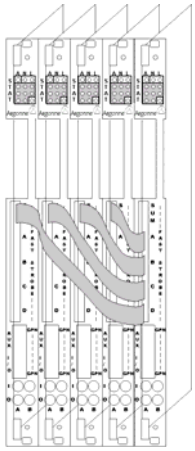

Figure 3 - ribbon cables from routers to master trigger (master at right of group)

The SUM connector is an output that has four possible settings based on a register in the CPLD. Table 1 provides the details. A master trigger's SUM output is normally not used; only routers use the SUM.

Setting	Data output on SUM connector (bits 7:0)			Expected Use
00 (default)	*Bit 7*	*Bit 6*	*Bits 5:0*	
	0	DISCBIT_OR	sum of coarse discriminator bits (DGS)	DGS router normal
01	*Setting 01 sends 8-bit data*			
	Sample of GRETINA-style LVDS bits direct from digitizers, links A-H			GRETINA compatible
10	*Setting 10 sends 8-bit data*			
	Sample of masked GRETINA-style LVDS bits direct from digitizers			GRETINA compatible
11	*Bits 7:0*			
	Diagnostic value from Threshold register			DGS router test mode

Table 1 - SUM connector output options

Comparison with GRETINA

In the GRETINA system, special CPLD firmware has been developed that generates the sum of the number of "central contact" discriminators active at any time, derived from the separate LVDS pairs of the SERDES cables, and outputs this on the SUM connector. As this sum can at most be eight as there are eight SERDES links from router to digitizer, not all the bits of the cables are required. A special set of "Y" cables has been produced, along with GRETINA-specific master trigger CPLD firmware, so that each of the input connectors A, B, C & D are viewed not as 8-bit numbers but instead as two 4-bit numbers from two different routers. In the GRETINA-specific master trigger CPLD, then, eight 4-bit sums are added together to form the fast multiplicity as opposed to the DGS case where four 8-bit sums are added.

Use of the separate LVDS bit

DGS digitizers have multiplexer logic that allows the separate LVDS bit on the SERDES cable to be driven from one of sixteen different signals, as shown in Table 2.

Selection from rj45 control register	Signal asserted on separate LVDS bit to router
0	Coarse discriminator bit from channel 0
1	Coarse discriminator bit from channel 1
2	Coarse discriminator bit from channel 2
3	Coarse discriminator bit from channel 3
4	Coarse discriminator bit from channel 4
5	Coarse discriminator bit from channel 5
6	Coarse discriminator bit from channel 6
7	Coarse discriminator bit from channel 7
8	Coarse discriminator bit from channel 8
9	Coarse discriminator bit from channel 9
10	OR of coarse discriminator bits from channels 5-9 (any Ge Center coarse)
11	Pileup-mediated (late) discriminator bit from channel 0
12	Timestamp based signal occurring at ~1.5kHz
13	Manual signal from pulsed control register
14	Fixed 0 for testing purposes
15	Fixed 1 for testing purposes

Table 2- DGS digitizer separate LVDS selections

Utility of the LVDS bit logic in DGS

Generally the SUM connector of the CPLD is configured to send the sum of the coarse multiplicity bits plus the DISCBIT_OR to the master; a common setting for the digitizers is to set the separate LVDS bit to selection 10 so that the "OR-of-ORs" option in the master becomes "Ge coarse multiplicity > 0" and then the multiplicity sum in the master becomes "Ge coarse multiplicity > threshold". This allows the end user to switch between two multiplicity comparisons for the FAST_STRB output with a single register access.

Alternatively, it is possible to select any single digitizer channel in the system by using the Mask registers of the routers to only allow the LVDS bit from one digitizer to participate and additionally setting the LVDS bit selection of that digitizer to a single channel. In this way any single channel may drive the DISCBIT_OR logic and be used as the source of the FAST_STRB trigger selection in the master trigger. This may be used to test each channel's response or to connect a special signal for coincidence purposes.

Finally, use of selection 11 provides a method by which the latency of the SERDES link from each digitizer back to the trigger may be measured. Since the pileup-mediated discriminator is the same signal as sent over the SERDES link for SumX and SumY triggers (including the Clean/Dirty logic in DGS), this selection provides a fast parallel path that generates a separate trigger through the FAST_STRB signal. Comparison of the timestamps issued in SumX (Y) triggers relative to FAST_STRB triggers from the same channel measures the trigger latency for the current settings.

Use of the Mask register in the router versus the master

In the router, the purpose of the Mask register is to provide bit-by-bit control over which of the separate LVDS inputs are ORed together to generate the DISCBIT_OR signal. This is required because the internal bias of the LVDS transceiver used to receive these signals reads an unconnected input as '1'. Each bit of the mask register corresponds to one LVDS bit. Setting the bit in the Mask register *enables* the LVDS bit to be part of the OR.

In the master trigger, the purpose of the Mask register is to select which of input connectors A, B, C & D are active in forming the total multiplicity sum. The lower four bits of the register correspond to the four connectors in order and the upper four bits are not used. Setting the bit in the Mask register *masks (disables)* the information from the selected connector. Yes, this is the opposite sense of the masking logic of the router, but is done to match the Masking is required because the buffer chips used have bus-hold circuitry that results in open connectors reading as if bits were still set.

Obviously these two usages are incompatible with each other, but as the separate LVDS bits are not connected between master and router there is no possible use of the logic associated with these bits in a master. Similarly the A,B,C & D cable inputs of a router are also not connected, and thus the apparent conflict is resolved.

Use of the Threshold register in the router versus the master

Since only the master uses the threshold register to define the multiplicity level, in the router the Threshold register may be used for other purposes. In the router, the Threshold register is re-purposed to provide the source of the user-defined diagnostic sum for test purposes. As previously seen, the SUM output connector of a router may be set to drive the current value of the THRESH register as a user-defined value. This may be used to statically test that the ribbon cables are properly connected and to verify the addition process in the master trigger.

To allow for some flexibility and automation of testing, one of the register addresses normally used only for a read-only operation has been configured to increment the value of the Threshold register by one each time the read-only register is written.

CPLD register I/O

Eight registers are implemented in the CPLD. Although VME cycles to the trigger module are A32/D32 for compatibility with the digitizer module, only the lower 16 bits of the VME data are actually used to communicate with the main FPGA. Similarly, the CPLD has a restricted width data connection, in this case due to a lack of pins in the CPLD. All data transfers to/from the CPLD are A32/D32 cycles but only the lower eight bits of the data are valid.

CPLD Register Addressing

A similar lack of pins for the CPLD requires careful interplay between the VME decoder FPGA, the main FPGA and the CPLD to define the addresses used by the CPLD. A second problem driven by software errors in the Python scripts generating the EPICS database requires that the addresses be limited to those below 0x8000 relative to the base address of the trigger board. Because of these limitations only a partial decode is used and the CPLD registers are scattered well apart from each other, but also appear at duplicate addresses.

CPLD A Connector Masked Status (read only) : Address 0x4000 and also 0x8000
CPLD B Connector Masked Status (read only) : Address 0x4004 and also 0x8004
CPLD C Connector Masked Status (read only) : Address 0x5000 and also 0x9000
CPLD D Connector Masked Status (read only) : Address 0x5004 and also 0x9004

BIT =>	7	6	5	4	3	2	1	0
RO	0	A	Masked sum					

BIT DEFINITIONS

- Bit 7 of the register is unused and always reads 0.
- Bit 6 reads the masked value of the Ge-center OR as sent from the router (bit 6 on ribbon cable).
- Bits 5:0 read the masked value of the Ge-center coarse partial sum as sent from the router.

GENERAL NOTES

- There are four registers, identically formatted, for each of connectors A, B, C & D.
- Bits 15:8 are unconnected and always read 0xFF.
- Bits 6:0 are controlled by the Mask register. If the connector is masked, bits 6:0 will read 0 irrespective of the bits on the ribbon cable.

CPLD Mask Register : Address 0x6000 and also 0xA000

Usage Model	BIT =>	7	6	5	4	3	2	1	0
Master trigger	RW	Unused				Conn D	Conn C	Conn B	Conn A
Router trigger	RW	Link H	Link G	Link F	Link E	Link D	Link C	Link B	Link A

BIT DEFINITIONS

- Bits 7:0, if ***set,*** enable the separate LVDS line from the given SERDES link to be used in the fast OR logic (typical in a router).
- Bits 3:0, if ***clear***, allow the given front panel connector's partial sum to be used in the full fast multiplicity sum (typical in a master).

GENERAL NOTES

- There is only one Mask register, but the register has two dissociated functions based upon whether the board is a master or router.

CPLD Mux/Discbit Register : Address 0x6004 and also 0xA004

Usage Model	BIT =>	7	6	5	4	3	2	1	0
ON WRITES (mux control)		FAST_STRB Control						SUM Conn Control	
ON READS (masked discbits)		Link H	Link G	Link F	Link E	Link D	Link C	Link B	Link A

BIT DEFINITIONS *when reading*

- Each bit reads back the status of the masked separate LVDS bit from each SERDES link. This is a live reading, not latched in any way, so if the LVDS bits are being driven by something that changes all the time the value will vary.

BIT DEFINITIONS *when writing*

- Bits 7:6 control the multiplexer that selects what signal will drive the FAST_STRB bit to the main FPGA.
    - If "00" (the default power-up state), the "OR-of-ORs" bit is provided to the main FPGA. This effectively provides a "multiplicity > 0" signal based upon the data presented to connectors A,B,C & D.
    - If "01", the FAST_STRB bit is asserted if the sum of the partial multiplicity sums presented to connectors A,B,C & D is greater than the value in the Threshold register of the CPLD.
    - If "10", the DISCBIT_OR signal drives the FAST_STRB. In this case the FAST_STRB is asserted to the main FPGA if the OR of all the masked separate LVDS bits is nonzero.
    - If "11", the FAST_STRB is driven high all the time (for testing purposes only).
- Bits 1:0 control the multiplexer that selects what data value will be sent out the SUM connector of the trigger module. See Table 1 above for the selections.
    - Setting "00" is that normally used by a DGS router to send partial multiplicity sums to the master trigger.
    - Setting "01" sends the unmasked separate LVDS bits over the ribbon cable and is usually only used for testing purposes.
    - Setting "10" sends the masked separate LVDS bits over the ribbon cable and is intended to emulate GRETINA router CPLD usage.
    - Setting "11" sends a bit pattern based on a counter and is designed for testing purposes.

GENERAL NOTES

- There is only one register here, but the register has two dissociated functions based upon whether you read or write it. On a ***read*** the masked set of separate LVDS bits is read back. On a ***write*** the multiplexers for the FAST_STRB signal to the main FPGA and the SUM output connector are set.
- Yes, this means that you cannot read back the values written for the multiplexer controls.

CPLD Threshold Register : Address 0x7000 and also 0xE000

BIT =>	7	6	5	4	3	2	1	0
RW	Multiplicity threshold							

BIT DEFINITIONS

- The register holds the multiplicity threshold that is compared against the sum of the masked partial sums received on connectors A,B,C & D. If the sum of the masked partial sums is greater than the threshold the comparison bit is set.
    - If the Mux register has bits 7:6 set to "10", the comparison bit is driven to the main FPGA as the signal FAST_STRB and may be used for triggering or to drive a NIM output.
    - If the Mux register has bits 7:6 set to any other value the comparison bit ("fast_mult") is unused and the value in the Threshold register is immaterial.

CPLD Multiplicity Sum Register (read only) : Address 0x7004 and also 0xE004

Usage Model	BIT =>	7	6	5	4	3	2	1	0
ON WRITES (increment THRESH register)	W	Value is immaterial							
ON READS (multiplicity sum)	R	Current total multiplicity sum							

BIT DEFINITIONS *on Reads*

- The register reads back the current total multiplicity sum as derived from adding together the partial sums expected to be available on connectors A,B,C & D. This register is intended to be only valid in the master trigger.
    - Note that this value is only valid if the cables are connected and the router triggers have had their Mux register set so that partial sums are being driven to the master.

BIT DEFINITIONS *on Writes*

Any write to this register address will increment the value in the Threshold register by one. The data being written is immaterial and does not affect the operation of the write cycle.