Digital Gammasphere &
Gamma Ray Energy Tracking In-Beam Nuclear Array

Trigger Timing and Control Link Specification

-- PRELIMINARY --

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All revisions after August 4, 2006 by J. Anderson

Document #TBA

1. OVERVIEW

This document describes the Trigger Timing and Control Link (TTCL) by which timestamps, trigger messages, and system-wide commands are shared between trigger and digitizer modules within the Gamma Ray Energy Tracking In-Beam Nuclear Array (GRETINA), Digital Gammasphere (DGS), Digital Fragment Mass Analyzer (DFMA) and MAJORANA triggering systems. DFMA is a multi-detector system supporting the Fragment Mass Analyzer, the Parallel Plate Avalanche Counter (PPAC) and the Dual-Sided Silicon Strip (DSSD) detectors. The specification described here is general and may be expanded to support additional detectors, augmenting any of the systems mentioned above. Physically the TTCL is transmitted from one module to another over a 1 gbps serial link using a serializer/deserializer (SERDES) chip.

The TTCL is generated in the Master Trigger of each system, and is propagated down through Router Triggers to the Digitizers. Together, the Master and Router Trigger modules comprise the cornerstone of the Trigger Timing & Control System (TTCS). In addition to the Masters and Routers, the TTCS may or may not also contain one or more Multi-purpose gamma Ray Interface to Auxiliary Detector (MγRIAD) modules. A special board, the Gammasphere Interface to Trigger Module (GITMO), provides a way to distribute clocks and triggering information from the master trigger crate of the original ("analog") Gammasphere system to the Master Trigger of Digital Gammasphere.

The MγRIAD board propagates the TTCL to auxiliary detectors and allows two way trigger message communication with the rest of the trigger system. The MγRIAD is considered to exist at the same level of the triggering hierarchy as a Master Trigger, with the primary difference being that a MγRIAD has only a single connection to the TTCL and thus may not re-propagate the TTCL beyond itself.

2. PHYSICAL SPECIFICATION

2.1 Master and Router Trigger

Hard metric (2mm pitch, IEC 61076-4-101) connectors and matching twisted pair cable sets with 100 ohm characteristic impedance are used throughout.

The typical physical implementation of the TTCL is intermingled with that of the Trigger Data link. An obvious choice, as the normal system connections require one of each between each front end board and the TTCS, it also makes sense in terms of the connector design. IEC 61076-4-101 connectors utilize a 5-row design that, at the front panel, allows for insertion of dual-twisted-pair connectors using the following pinout:

Row #	Link Name	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Function
25	A	LVDS IO +	LVDS IO +	GND	LVDS IO +	LVDS IO +	
24		Data In +	Data In -	SHLD	TTCL Out -	TTCL Out +	Data In / TTCL Out
23	B	LVDS IO +	LVDS IO +	GND	LVDS IO +	LVDS IO +	
22		Data In +	Data In -	SHLD	TTCL Out -	TTCL Out +	Data In / TTCL Out
21	C	LVDS IO +	LVDS IO +	GND	LVDS IO +	LVDS IO +	
20		Data In +	Data In -	SHLD	TTCL Out -	TTCL Out +	Data In / TTCL Out
19	D	LVDS IO +	LVDS IO +	GND	LVDS IO +	LVDS IO +	
18		Data In +	Data In -	SHLD	TTCL Out -	TTCL Out +	Data In / TTCL Out
17	E	LVDS IO +	LVDS IO +	GND	LVDS IO +	LVDS IO +	
16		Data In +	Data In -	SHLD	TTCL Out -	TTCL Out +	Data In / TTCL Out
15	F	LVDS IO +	LVDS IO +	GND	LVDS IO +	LVDS IO +	
14		Data In +	Data In -	SHLD	TTCL Out -	TTCL Out +	Data In / TTCL Out
13	G	LVDS IO +	LVDS IO +	GND	LVDS IO +	LVDS IO +	
12		Data In +	Data In -	SHLD	TTCL Out -	TTCL Out +	Data In / TTCL Out
11	H	LVDS IO +	LVDS IO +	GND	LVDS IO +	LVDS IO +	
10		Data In +	Data In -	SHLD	TTCL Out -	TTCL Out +	Data In / TTCL Out
9	L	GND	GND	GND	GND	GND	Interlink shield
8		TTCL In +	TTCL In -	SHLD	TTCL Out -	TTCL Out +	TTCL In / TTCL Out
7	R	GND	GND	GND	GND	GND	Interlink shield
6		TTCL In +	TTCL In -	SHLD	TTCL Out -	TTCL Out +	TTCL In / TTCL Out
5		GND	GND	GND	GND	GND	Interlink shield
4	U	GND	GND	GND	GND	GND	Interlink shield
3		TTCL In +	TTCL In -	SHLD	TTCL Out -	TTCL Out +	TTCL In / TTCL Out
2		GND	GND	GND	GND	GND	Interlink shield
1		GND	GND	GND	GND	GND	Interlink shield

Table 1: Master/Router front panel pinout.

The SERDES links are shown in white. In this cartoon, 'GND' indicates connection to ground, 'SHLD' to a shield common to the two pairs, and the '+' and '-' indicate the wire pairs themselves.1 This "wafer" is how the cable assemblies are manufactured. Multiple wafers may be stacked upon each other to make larger cables. In the case of this link, one twisted pair of each "wafer" may be used for the TTCL, and the other used for the Trigger Data link to make a

[1] Whether "ground" and "shield" are the same or not depends upon the choice of wafer end on the cable, the choice of connector used on the printed circuit board and the design of the circuit board itself.

most convenient assembly. The usual front panel connector provides connectivity for 22 or 25 of these "wafers" in one unit, with polarization and strain-relief clips part of the standard.

2.2 Digitizer, Digitizer Tester, GITMO and MγRIAD

The Digitizer, Digitizer Tester, GITMO and MγRIAD only have one bi-direction SERDES link each, and therefore do not require the relatively high density IEC 61076-4-101 connector. Instead they provide a single port using an RJ45 connector. This is the same connector as is used for wired Ethernet, but the TTCL ***is not Ethernet and is not physically compatible with Ethernet***. No termination is built into the connector itself. Any requires termination is handled by discreet passives on the PCB itself. The pinout of this connector is shown below:

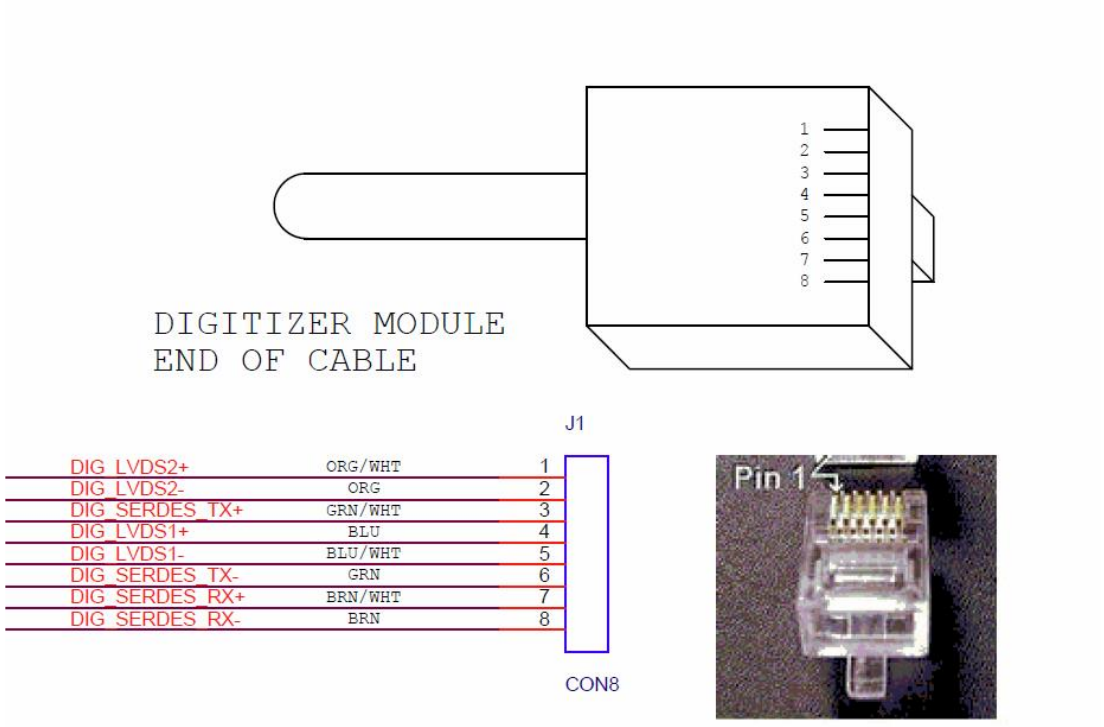

Figure 1 - Pinout of RJ-045 connector to Digitizer, Digitizer Tester, GITMO, and MγRIAD.

The TTCL is propagated to the digitizers on the SERDES RX+/-. The Trigger Data Link is sent by the digitizer to the trigger system on the SERDES TX+/-. Lines LVDS1 and LVDS2 are auxiliary LVDS signals that normally are defined as flowing from the digitizer to the trigger system. In the GRETINA implementation, one is used as a fast copy of the discriminator from one channel used for multiplicity triggers and the other is a 'throttle request' asserted when the digitizer's FIFO is becoming full. In DGS, the 'throttle request' is used in the same way as GRETINA, but there is no defined use for the other line. The usage and direction of these auxiliary lines is dependent upon the needs of a given experiment and the versions of firmware (trigger and digitizer) in use.

3. ELECTRICAL SPECIFICATION

The TTCL is a high speed link. With a bit rate of 1Gbps and edge transition times in the 100psec range, very careful attention to high speed signaling concerns is paramount. This section will provide some basic information to assist designers and users in coping with these concerns.

3.1 Chipset

The commercial chipset selected for this communications link utilizes the National Semiconductor DS92LV18 as the SERDES, with the National Semiconductor DS90LV004 cable driver/receiver providing the physical interface between the SERDES and the cable itself.

3.1.1 Timing Information

A 50.000MHz clock is used as the master parallel word input clock. Thus, the serial bit stream on the cable will run at twenty times that clock rate, or a rate of 1Gbps. At these frequencies, proper printed circuit board layout, connectors, cables and termination are all critically necessary to insure proper operation.

3.1.2 Distribution of System Clock

The clock edge transitions buried in the serial data in the two "extra" bits transmitted between bit 17 of word *n-1* and bit 0 of word *n* are used by the SERDES receiver chip to regenerate a clock that matches the frequency and is at fixed (and minimal) phase offset relative to the parallel word clock used to load the command frames. The phase locked loop of the receiver has a relatively wide capture range and can follow ±5% variations in frequency if the rate of frequency drift is slow relative to the period of the clock itself. Thus, the onus is on the master trigger board to have a low drift, phase stable initial source clock to insure that the system as a whole does not wander.

In a large system such as the mixed DGS/DFMA system accumulative clock jitter over many 'hops' of the TTCL can result in significant data errors at the far end. At 1Gbps serial line rate a total accumulated jitter of less than 250ps at the far end is strongly recommended. To achieve this over a large system will typically require strong filtering of power supply noise on each board's clock multiplexer that switches between the local oscillator and the received clock from the SERDES link so that the accumulated jitter per board is less than 50ps.

3.2 LVDS signal levels

The chipset selected for the TTCL uses Low Voltage Differential Signaling (LVDS) technology. This circuit architecture uses current steering to create 1s and 0s by driving a current one way or the other in a pair of conductors, developing voltage across a terminating resistor at the end of the line. The standard has been extended to use in bussed applications, but it was originally designed for, and it still best used in, point-to-point applications such as the TTCL.

In normal usage the transmission line is chosen to have an odd-mode characteristic impedance of 100 ohms, and a 100 ohm resistor is used across the conductor pair as the terminator. With typical LVDS currents (5mA), this generates a differential voltage of about 500 millivolts at the input of the receiver. Shielded cables and/or the use of pre-emphasizing drivers, is typically required for cable lengths in excess of 10 meters.

3.3 Printed Circuit Board layout considerations

The high speed of the system requires that differential traces on printed circuit boards be very well matched. Vias and package pins have to be viewed as potentially self-resonant circuits. Even the mismatch in the length of right-angle connector pins becomes a concern; this means that if the 'blue' conductor of a twisted pair in board 'a' has the longer connector pin path, the *other board at the other end of the line* has to be designed such that the 'red' conductor of the twisted pair gets the longer path. Boards cannot be developed in isolation – the designers at both ends of the cable must work together. Chapter 3 of National Semiconductor's "LVDS Owners Manual" (found at http://www.national.com/appinfo/lvds/files/lvds_ch3.pdf) is a good general reference. If a copy of the MECL System Design Guide from Motorola can be found, it is also a good reference work, especially chapter 7.

4. SYSTEMS THAT USE THE TRIGGER & TIMING CONTROL LINK

4.1 GRETINA

The GRETINA electronics system is described in GRETINA document #GRT-3-060412, "GRETINA Electronics System". That document contains an overall cartoon of the electronics system, copied here as Figure 2: Overview of front panel connections in the GRETINA system..

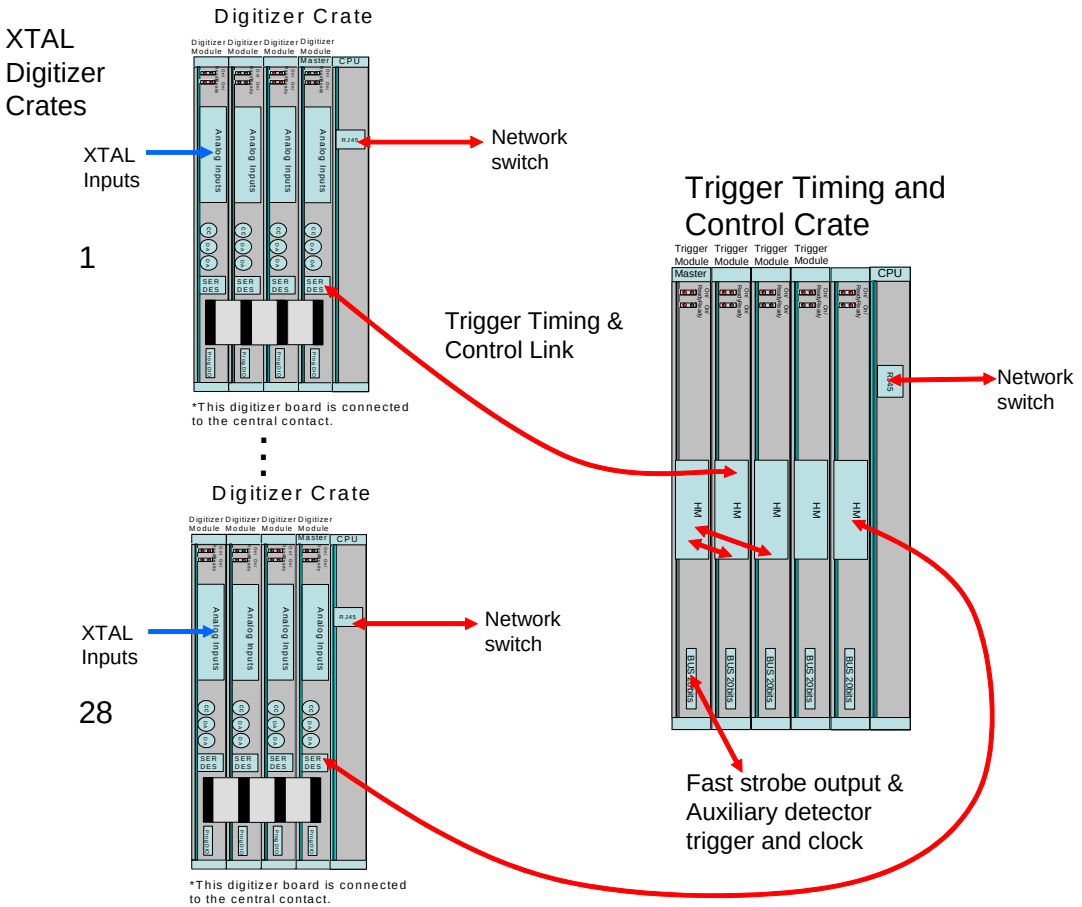

Figure 2: Overview of front panel connections in the GRETINA system.

4.1.1 Hierarchical trigger implications - GRETINA

The TTCS is assumed to consist of one Master trigger module with a tree structure of subsidiary "router" or "slave" trigger modules. All information sent over the TTCL is originally sourced by the master trigger unit. Subsequent layers of trigger modules shall receive and retransmit the commands without modification or response except where noted otherwise below. Figure 3: TTCS interconnection hierarchy. shows the structure of the trigger hierarchy for GRETINA.

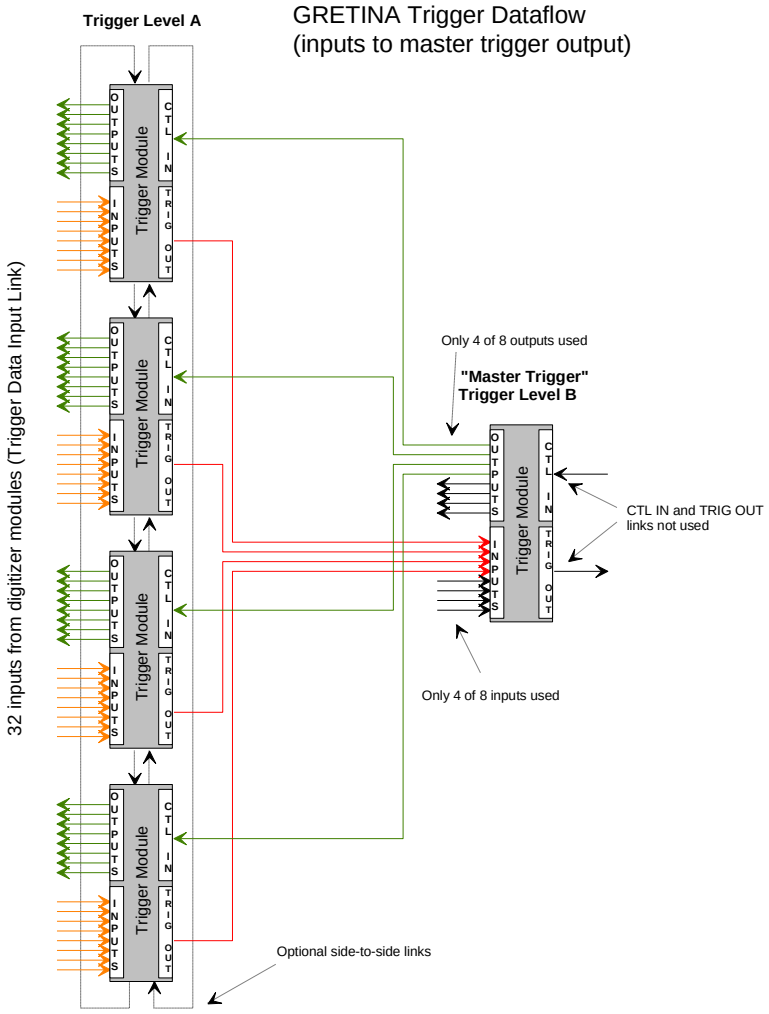

Figure 3: TTCS interconnection hierarchy.

This hierarchical organization is expansible from the GRETINA implementation to one usable for the full GRETA detector. Figure 3 shows how a third layer may be added to implement a TTCS usable for 128 front end digitizers and defines all the various links associated with the TTCS by name.

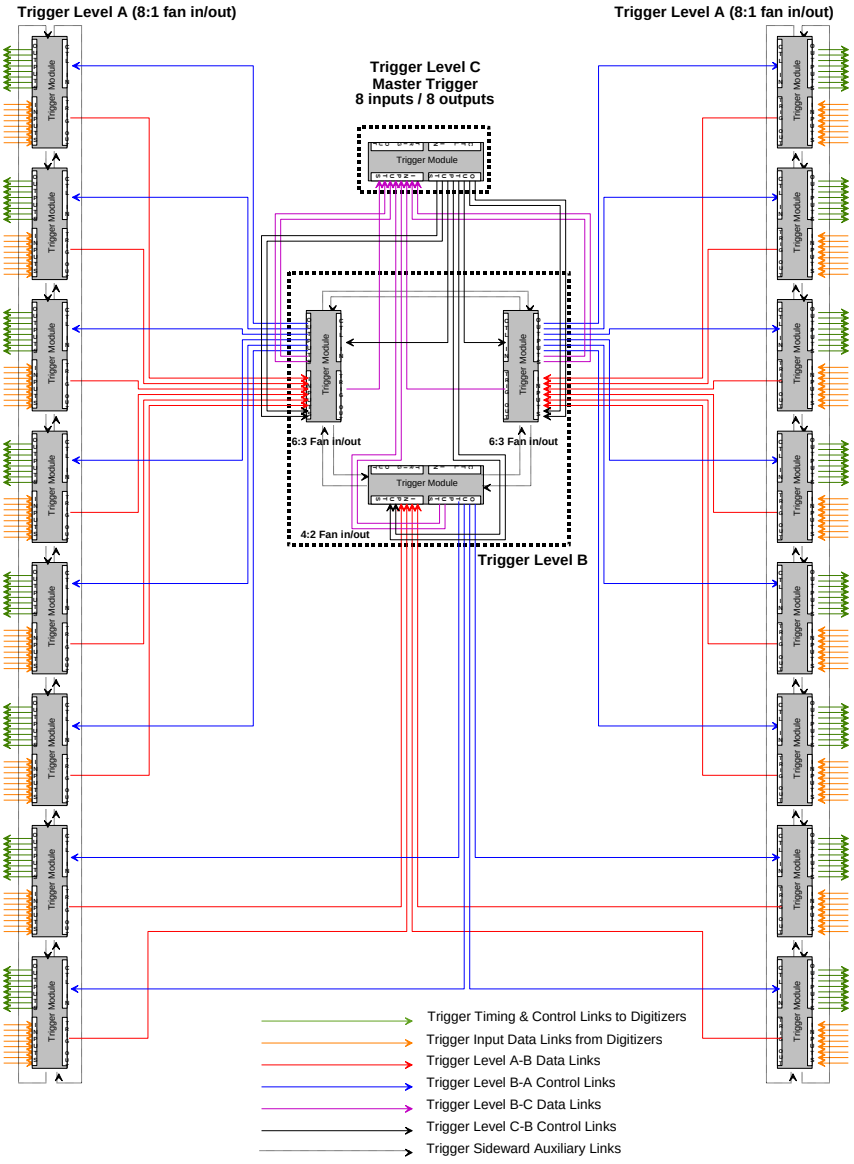

Figure 4: Expansion of TTCS for full GRETA implementation

4.2 DGS/DFMA

Figure 5: Overview of the DGS/DFMA system. shows a basic cartoon of how the Trigger and Digitizer modules connect to each other in both DGS and DFMA. Both DGS and DFMA implement their own DAQ, but triggering and timing are common.

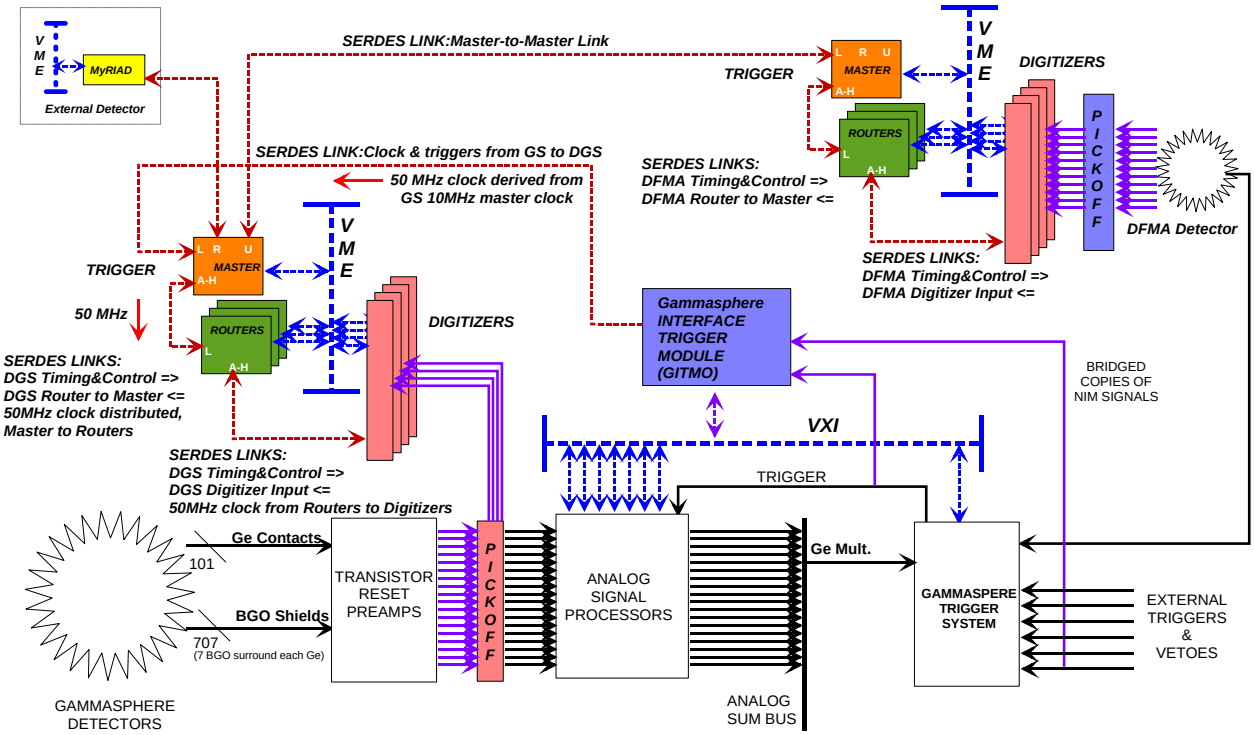

Figure 5: Overview of the DGS/DFMA system.

A number of trigger-like modules other than the Master and Router exist in the Digital Gammasphere/DFMA system that must be defined at this juncture. It is important to note the specific link names (A-H, L, R and U) in Figure 5, shown in white lettering.

- The GITMO picks off signals from "Analog" Gammasphere and, via SERDES link, provides auxiliary trigger signals and a reference clock to the Master Trigger. The data format of the GITMO is not compatible with the TTCL and is specific to the DGS implementation. The Master Trigger firmware for DGS assumes that any connection to link L is from a GITMO. The Master Trigger firmware for DFMA is more general in that it assumes that any connection to link L will transmit in TTCL format.
- The MγRIAD is a module that provides additional auxiliary detector trigger connectivity to a Master Trigger, and may be used to propagate timestamps and triggers to other VME-based data acquisition systems that don't use digitizer modules. The MyRIAD may also monitor the operation of external, non-TTCL trigger systems in other detectors through NIM or ECL signals, and transmit trigger messages back to the Master Trigger. The MγRIAD both sends and receives in TTCL format. A MγRIAD is normally connected to link R or U of a Master Trigger.

- The Digitizer Tester (not shown in Figure 8) is a test stand module that listens to the Trigger Timing and Control SERDES link and generates test waveforms to exercise digitizers. It is not normally part of a detector system but may be used within one to emulate most waveforms generated by particle detectors including pileup.

4.2.1 Hierarchical trigger implications – DGS/DFMA

The TTCS is assumed to consist of one Master trigger module with a tree structure of subsidiary "router" or "slave" trigger modules. The DGS and DFMA systems are *independent* hierarchies that allow *selective propagation* of clock and trigger information between them (see section 7.3.4). Within the two systems, all information sent over the TTCL is originally sourced by the master trigger of that system. Figure 6 shows the structure of the trigger hierarchy for DGS and DFMA. Up to eight Routers per Master may be used.

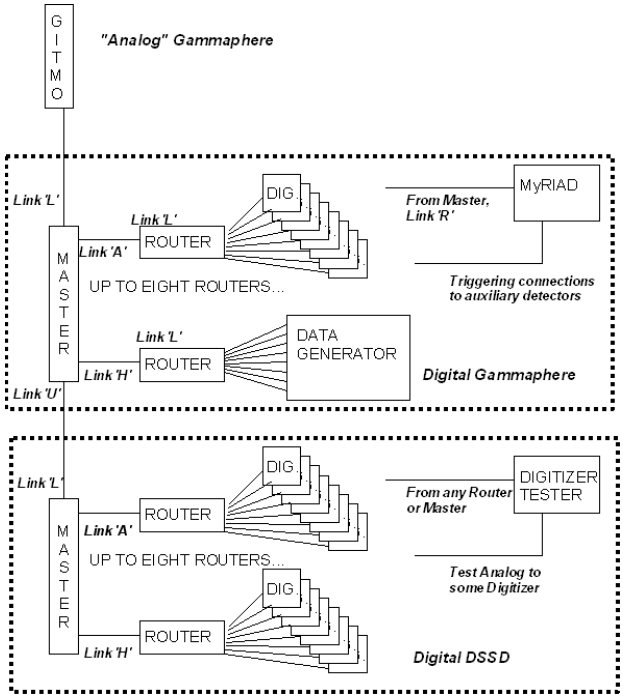

Figure 6: Trigger Timing & Control System interconnection hierarchy.

4.3 Selective Propagation Concept within DGS/DFMA

A new TTCL feature introduced with the development of firmware for DGS/DFMA is that of ***Selective Propagation.*** This feature defines what portions of the TTCL data received by a Master Trigger module over links L, R and U is allowed to propagate into the 'local domain' of a given Master Trigger from the "outside world". An obvious use of selective propagation is to allow some subset of Trigger Decision messages from one Master to propagate into the domain of another; by this technique, detectors are allowed to cross-trigger each other, assuming that the clocks and timestamps of each have been correlated. The details of Selective Propagation are provided later in this document after the protocol has been defined.

5. THEORY OF OPERATION

The TTCL provides the method by which the TTCS controls and synchronizes the operation of the digitizers and any auxiliary detector systems. The exchange of information between the master trigger module and other devices is synchronous and the master trigger module determines the synchronization. A synchronous implementation is easier to implement and maintain. The master trigger sends a command every 100 nsec (five words at 20nsec/word). A series of twenty command frames (100 words, five words per frame) will be referred to hereafter as a "system cycle". The trigger repeats the trigger cycle endlessly. Each of the twenty frames within a trigger cycle either causes an action in the system or is null (specific null frame, defined below). The entire system cycle takes (20 * 0.10us), or 2 microseconds, to complete.

The repeating system cycle allows the TTCS to regularly synchronize activities at the front end while still providing plenty of extra command frames to slip in asynchronous needs (system reset, initialization, status requests, etc.) as necessary.

5.1 Dissection of the System Cycle

The twenty command frames comprising a trigger cycle are, for the most part, pre-defined. Some command frames will *always* occur every trigger cycle to insure synchronous operation of the system. Other frames are *optional*; they only occur if there is a reason to issue them within this particular cycle. If an optional frame is not required, a *null* frame (identified by a unique Command Byte) is issued. By caveat, no front end device may respond in any way to a null command frame. Certain cycles are *reserved* for future expansion or internal trigger use. Front end designers shall assume that these cycles will transmit null commands to the front ends unless superseded by later revisions of this document.

5.2 System Cycle Breakdown

A few overall timing notes are in order at this point:

1. A Sync Frame is issued every 2 microseconds. These frames provide overall system synchronization.
2. Trigger decision frames always occur at the same times in each trigger cycle. This determinism is to aid in debugging the system. In each trigger cycle (2 microseconds) up to eight triggers may be issued. The number of triggers the TTCS will issue in a trigger cycle is latched prior to the beginning of the cycle. If a trigger decision "just misses" it will be delayed two microseconds.
3. Data input via the Trigger Data link is also synchronized on a two microsecond clock via this command structure. The presumption is that the Trigger Data link contains both "fast" and "slow" data. "Fast" data is constantly transmitted, but "slow" data is only sent in response to a command demanding it, as issued by the TTCL.

5.3 System Timestamp

The TTCS maintains a 48-bit counter, incremented every 10nsec (100MHz), that is referred to as the System Timestamp. The value of this counter is regularly broadcast to all front end electronics to provide event synchronization information. Since the serial communications hardware used to carry the information has a word rate of only 50MHz, the Trigger system shall

internally synchronize the data sent on the serial link such that words are only loaded when the 100 MHz System Timestamp is an *even* number (the LSB is zero). Receivers of the Trigger Timing and Control link shall synchronize any clock multipliers such that any master timing counter run from a 100MHz clock, synthesized from the 50MHz word clock from the physical link, is constrained to have its LSB equal to zero immediately following those rising clock edges that are coincident with the rising edge of the physical link's word clock.

5.4 DGS and DFMA timestamp correlation

Digital Gammasphere uses the same Trigger and Digitzer modules as in the GRETINA experiment, but with significantly modified firmware. The system at Digital Gammasphere contains two data acquisition systems, DGS and DFMA. Major additions to the GRETINA version of the TTCL have been made that allows the two systems to cross-synchronize to each other, cross-trigger each other plus share the same clock and timestamp.

5.4.1 Clock synchronization with Analog Gammasphere in DGS

The Gammasphere Interface Trigger Module (GITMO) provides a link between the existent legacy trigger system of "Analog" Gammasphere and the digital data acquisition of Digital Gammasphere. The GITMO sends a continuously repeating sequence of data words indicative of the trigger state of "Analog" Gammasphere, allowing the DGS system to trigger whenever "Analog" Gammasphere triggers. Because a SERDES link is used, the DGS Master may lock onto the clock from that data stream and run synchronously to the clock from "Analog" Gammasphere; while timestamps are generated independently the use of the same clock frequency allows direct timestamp comparison between the legacy and the new system.

6. PROTOCOL SPECIFICATION

The TTCL protocol consists of three trivial layers: Words, Frames, and Cycles. There are 20 bits in a word, 5 words in a frame, and 20 frames in a cycle. Each system cycle begins immediately after the previous. Data cycles continuously until the link is disabled by some means.

6.1 Word Format

The DS92LV18 sends data in 20 bit words. Two of these are generated internally by the DS92LV18 to embed the serialization/deserialization clock and cannot be used for data. Bits 17 and 0 have been designated for special use, leaving 16 bits of payload, as show below. From this point forward all frames will be defined solely in terms of the 18-bit payload that firmware generates and responds to.

Bit	**A**	**17**	**16..1**	**0**	**B**
'Value' Field Name	'0' Embedded clock edge	'0' "Edge Guard"	Data Payload	'0'/'1' Polarity Flag	'1' Embedded clock edge

Table 2: Word format.

6.1.1 Embedded Clock

The command frames are sent over a commercial Serializer-Deserializer (SERDES) chipset that converts the 18-bit parallel words into 20-bit serial bit streams (the extra two bits embed the system clock transitions). Bit 17 of the parallel word is transmitted adjacent (immediately prior) to the system clock transition in the serialization process; by fixing it at '0', it acts as a guard bit to insure the reliable recovery of the system clock at the receiving end.

6.1.2 DC Balance

The TTCS modules, may calculate the disparity of each command frame's words by counting how many 1s and 0s are in each word. On a word by word basis the TTCS may either send "true" or "invert" data in bits 16..1 to maintain the best overall bit disparity ratio. Bit 0 is used as a polarity flag to allow for DC balance considerations on the physical interconnection. If '0', the data in bits 16..1 are *inverted* and should be re-inverted upon receipt. If bit 0 is '1', all data is correct as received.

6.1.2.1 Compatibility Requirements

All modules must implement logic to receive DC balanced data. Modules are not required to support transmitting DC balanced data.

6.2 Frame Format

The TTCL consists of an endlessly repeating series of command frames. Each command frame is composed of five eighteen-bit words, in the following order.

Word	Bit 17	Bits 16..9	Bits 8..1	Bit 0
1	0	Command Byte	Command Argument	Polarity Flag
2	0	Auxiliary Information	Auxiliary Information	Polarity Flag
3	0	Auxiliary Information	Auxiliary Information	Polarity Flag
4	0	Auxiliary Information	Auxiliary Information	Polarity Flag
5	0	Auxiliary Information	Auxiliary Information	Polarity Flag

Table 3: TTCL Frame Format

6.2.1 Command Frame Structure

Each command frame consists of five words. The first word contains the command byte and any auxiliary information necessary to modify the command itself. The front-end digitizer boards (or any other front-end module) receive the command frames and respond as required by decoding the Command Byte and the Command Argument. The second through fifth words of the frame are the data associated with the command. The Auxiliary Information is command dependent; details are in subsequent sections. The use of a Command Byte and a Command Argument in the first word is not strict; the entire 16-bit word may be used as a single Command.

6.2.1.1 Null Commands

If a given command frame has no command to send, the frame's data will consist of the Null Command Frame. This is shown below:

Word	Bits 16..1
1	0xAAAA
2	0xAAAA
3	0xAAAA
4	0xAAAA
5	0x0000

Table 4: Null command format.

6.2.2 GRETINA Defined Command Byte Values – summary table

The table below shows a list of command bytes associated with specific actions. However, it is important to note that the command in any given frame is dependent on the index of that from within the system cycle. The actual set of valid commands for a given frame may include values not shown in the table below. See later sections of this document for details on each command frame.

Command Byte Value (hex)	Meaning of Command
0x00	Null command – do nothing
0x01	Sync (check timestamp)
0x02	Debugging Control Command
0x04	Front end calibration inject
0x08	Latch Status & Monitoring Data
0x10	Front End Reset
0x18	Front End Reset (serial links only)
0x22	Added 20160418 for a Digital Gammasphere “External Discriminator Request”
0x40	Demand Front End Slow Data
0x50 – 0x5A, 0xA5	Trigger Decision Frame
0x81	Imperative Sync (force reload of timestamps)
0x90 – 0x97	Auxiliary Detector command (reserved)
0x98 – 0x9F	Main Detector Miscellaneous command (reserved)
0xAA	Null command – do nothing
0xFF	End-of-Cycle command (no action, timing cycle boundary marker only)

Table 5: Command byte values for specific commands.

If the command byte of any command frame received is an undefined value, the receiver should not process it, and should report an error. Such errors should be reported to the slow monitoring system, not to the TTCS.

6.3 Cycle Format

Table 6 shows the timing breakdown of one entire System Cycle. The various command frames listed therein are described in the following subsections. Italicized command frames are *mandatory*. They are always issued and may not be replaced by a null frame. All other frames will either contain the specified type of frame or a null frame, as required.

Frame number	Start Time, ns	End Time, ns	Purpose of Command Frame in GRETINA and MAJORANA	Purpose of Command Frame in DGS/DFMA
1	0	100	***Sync command***	
2	100	200	Debugging Control Command ***(may affect other commands within frame)***	Unused in DGS/DFMA; null frame.
3	200	300	Trigger Decision command	
4	300	400	Trigger Decision command	
5	400	500	Trigger Decision command	
6	500	600	Trigger Decision command	
7	600	700	Trigger Decision command	
8	700	800	Trigger Decision command	Selectively propagated Trigger Decision
9	800	900	Trigger Decision command	Selectively propagated Trigger Decision
10	900	1000	Trigger Decision command	Selectively propagated Trigger Decision
11	1000	1100	Spare (Null until defined otherwise)	
12	1100	1200	Internal trigger reserved frame (Null to all front ends)	
13	1200	1300	***Demand front end slow data command***	***Unused in DGS, but checked by firmware***
14	1300	1400	Unused, reserved frame	Internal trigger commands to Digitizer Tester
15	1400	1500	GRETINA Front End Asynchronous command (Calibration Inject, Latch Status or Reset)	Unused (null)
16	1500	1600	Unused (null)	Synchronous System Capture command
17	1600	1700	Auxiliary Detector Reserved Command (Null if not required)	
18	1700	1800	Spare (Null until defined otherwise)	
19	1800	1900	Spare (Null until defined otherwise)	
20	1900	2000	***End-of-Cycle command***	

Table 6: Frame by frame breakdown of trigger cycle.

6.3.1 Overview of frame usage

The various frames within the system cycle may be broken into a few simple categories.

- Frames 1 and 20 are used for receiver machine synchronization and propagation of the system timestamp.
- Frames 3-10 are used to transmit trigger acceptance messages that cause selection of events within the digitizer modules.
- Frames 12 and 14 are reserved for internal use within the trigger system.
- Frame 13 is used for a GRETINA-specific data synchronization function. DGS/DFMA digitizers do not use this command but require its presence and correct format.
- Frames 15, 16 and 17 are intended for sending occasional, non-repeating messages to various modules that may be connected to the trigger system, allowing for broadcast of slow control commands or synchronized control operations.
- Frames 2, 18 and 19 are unused (or effectively so).

6.4 Implementation of Selective Propagation (DGS/DFMA only)

The primary concern of selective propagation is the clock and the timestamp. A control bit in every module of every type in this system determines whether the module runs from its own internal oscillator or from a clock received from an external source. In the case of Trigger modules, an external clock may be received via Link L only. However, when multiple detectors with multiple Master Triggers are chained together (for example. DGS/DFMA), a method must be defined to specify which Master is the source of Imperative Sync commands.

Three registers are implemented in DGS/DFMA Master Trigger firmware:

- The Link L Propagation Control Register,
- The Link R Propagation Control Register and
- The Link U Propagation Control Register.

Bits within each register specify which *frames* of the TTCL data received from their associated link *may be propagated into the local system from a remote source.* At power-up, these registers all initialize to zero, so that no propagation of remote data is allowed. Each of the Propagation Control Registers is bit-mapped per-frame, as shown in Table 7. Each bit, if set, enables the propagation of information from the indicated frame.

Bit=>	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Name	F19	F18	F17	F16	F14	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F1

Table 7 – General format of a Propagation Control Register

6.4.1 Sync Command Propagation

The ‘F1’ bit is only active for the Link L Propagation Control Register. If the bit is set, then Imperative Sync commands received over Link L are propagated into the local system. If the bit is clear, only the local Master may assert Imperative Sync. Generally it is recommended that the F1 bit of each Master that receives a clock from another Master be set, so that there is a single module that can assert Imperative Sync throughout multiple detectors.

6.4.2 Trigger Command Propagation

The F3 through F10 bits, implemented in all three Propagation Control Registers, allow any subset of Trigger Decision frames from each link to be selectively re-propagated to the Routers and Digitizers of the local system. This allows for operation of multiple-detector experiments where the user may dynamically control which triggering conditions in each detector may cause triggers to occur *within other detectors.* As described in Section 7.3, re-propagated trigger decisions buffer up within their own FIFOs and are re-propagated during the last three Trigger Decision frames (Link L: Frame 8; Link R: Frame 9; Link U: Frame 10). To avoid the risk of deadly embrace, the command sequence sent out each of these three links (L, R, U) is coded so that a link may not re-propagate back the trigger decision frame assigned to itself.

6.4.3 Propagation of other command frames

Bits 15:9 of the Propagation Control Registers allow selective propagation of other command frames including frames currently defined as spares.

- The F11, F18 and F19 bits are reserved for future use in case any of these spare frames are assigned specific functionality that may require re-propagation.
- The F12 bit allows propagation of the Internal Trigger Frame (defined in section 7.5) from one detector to another. Generally the Internal Trigger Frame is used in test stands, rather than running experiments, so this bit is not often used.
- The F14 bit allows propagation of the Internal Trigger Frame defined in section 7.6.2. This is useful in experiments where one or more Digitizer Tester modules have been added to generate "fake events" in some digitizer channels correlated to specific timestamps.
- The F16 bit is expected to be the most commonly used propagation control bit other than the F1 bit. When set, this bit allows re-propagation of the Synchronous System Capture Command defined in section 7.8. With propagation of this command enabled, a single over-arching Master (or "Monarch") may issue a single Synchronous System Capture Command and have it take effect throughout a multi-detector system.
- The F17 bit, if set, allows propagation of Auxiliary Detector commands (see section 7.9). Akin to the F16 bit, this allows control of auxiliary detector interfaces (MγRIADs) from a single top-level control point.

7. FRAME SPECIFICATION

The following subsections detail the exact structure of each frame and the commands that may be presented therein upon the TTCL.

7.1 Frame 1 – Sync Command

The Sync command's purpose is dual. It not only marks the beginning of the 2 microsecond system master timing interval, but it also commands all front end processors to compare their internal timestamp counter to the value sent with the Sync command. If a mismatch occurs, the front end should latch an internal status value indicating that it fell out of sync.

7.1.1 Sync / Imperative command

Word	Bits 16..9	Bits 8..1
1	0x01 (hex) or 0x81 (hex)	Rollover Notification
2	System Timestamp[47..40]	System Timestamp[39..32]
3	System Timestamp[31..24]	System Timestamp[23..16]
4	System Timestamp[15..8]	System Timestamp[7..0]
5	0x0000	

Table 8: Format of a sync command.

TTCS modules other than the master trigger shall perform internal checking of their timestamp count in response to this command as well, if they use the timestamp. The low order byte of the first word of the command indicates whether the System Timestamp has rolled over (count passed 0xFFFFFFFFFFFF). In normal operation this should never occur as it will take over 30 days for the System Timestamp to roll over, and it is expected that systemic resets will occur more frequently than this. None the less, for robust operation, a Rollover Notification is provided. If the System Timestamp has rolled over, the Rollover Notification will be set to 0xFF and shall stay that way until the timestamp reaches 0x000000010000. If no rollover has occurred or the timestamp has passed 0x0000000FFFF since the last rollover, the Rollover Notification byte shall be 0x00. Routers must synchronize to the timestamp and pass it on to all links (A-H, L, R and U).

In some cases (e.g., recovery from error, system startup, etc.), it may be imperative that the front end device reload the timestamp. An Imperative Sync command (0x81) is issued at these times by the TTCS. All front ends receiving an Imperative Sync shall reset their timestamps and buffer counts immediately upon receipt of this command, synchronous with receipt of the immediately following Command Byte of the next command.

When not running off the SERDES recovered clock, MγRIADS, Digitizers and Digitizer Testers must provide must provide their own, locally generated, timestamp.

7.1.2 Sync Command Expansions in DGS/DFMA

- The Link L Propagation Control Register in each master trigger controls whether the timestamp distributed by that Master is the locally generated timestamp or the remote Master's timestamp as received via Link L. As a sanity check, the Link L Propagation Control Register bit may not take effect unless the Link L SERDES is locked, the receiving state machine is locked to a command stream and the separate clock-source control bit is set.
- A Master Trigger shall provide registers that default on power-up to zero, but that may be changed by the user, to contain the timestamp value to be sent during an Imperative Sync.
- Router and Digitizer modules shall reset to the transmitted timestamp during an Imperative Sync and shall not assume that the timestamp resets to zero.

7.2 Frame 2 - Debugging Control Command

7.2.1 Debugging Control Command (command byte = 0x02)

The TTCS implements a buffer FIFO that may be filled from VME with arbitrary data. An internal VME register allows the slow control system to demand that the TTCS temporarily suspend normal TTCL operation and, instead, send out the information contained within the FIFO. When this occurs, the TTCS shall act in the following manner:

1. The current trigger cycle will complete normally and shall not be affected.
2. The immediately following trigger cycle shall issue the Sync command in frame #1, and then issue the Debugging Control Command in frame #2.
3. The following seventeen frames (#3 - #19) shall be derived from the first 85 words stored in the FIFO.
4. The End-of-Cycle command frame (#20) shall be issued in its normal format and position.
5. Following trigger cycles shall continue to be issued following steps 2-4 above until the FIFO is empty. When the FIFO empties, the trigger cycle will be filled with Null commands as necessary until the End-of-Cycle command frame is reached. The next frame after the FIFO empties will be normal.
    a. A provision may be provided to allow the FIFO to continuously recycle until the slow control system aborts the debugging mode.
    b. If recycling is allowed, the abort will occur synchronously with a trigger cycle so that no partial trigger cycles occur.
6. Any trigger decisions that were in the pipeline at the time Debugging was initiated will be aborted and the internal trigger pipelines will be cleared.
7. Similarly, Fast Strobe multiplicity counts shall also be cleared to zero at the time Debugging is initiated. A bit in the FIFO shall be logically ORed with the Fast Strobe decision during Debugging such that the Fast Strobe may be manually created during this mode irrespective of the actual multiplicity count.
8. The System Timestamp shall not be affected by entry into or exit from Debugging.

7.2.2 The Debugging Control Command in DGS/DFMA

The Debugging Control Command has been removed in DGS/DFMA and is re-defined as a Null frame.

7.3 Frame 3 through 10 - Trigger Decision Commands

Frames 3 through 10 are all identically formatted Trigger Decision Commands.

7.3.1 Trigger Decision command

Index	Bits 16..9	Bits 8..1
1	Trigger Type Code	Front End Selection
2	Event Timestamp[47..40]	Event Timestamp[39..32]
3	Event Timestamp[31..24]	Event Timestamp[23..16]
4	Event Timestamp[15..8]	Event Timestamp[7..0]
5	0x0000	

Table 9: Format of a trigger decision command.

When the master trigger module determines that an event condition meeting trigger criteria has been received, it issues the Trigger Decision command. Receipt of a Trigger Decision command by the front end is always a "positive" decision; no command is issued if an event doesn't meet the criteria. It is assumed that non-triggerable events will simply flush out of buffer memories in the front end devices, given sufficient time.

A Trigger Decision command carries with it a timestamp. This timestamp is *not* the current system timestamp, but instead marks the timestamp *of when the trigger system determined that a trigger had occurred.*

7.3.1.1 GRETINA-specific details

Dependent upon the type of trigger that is satisfied, the values of the Trigger Type Code and Event Timestamp sent are resolved in one of three ways:

- If the trigger decision is reporting a multiplicity trigger from the "fast" data (i.e., the Fast Strobe output of the TTCS has fired within the last two microseconds), then the Event Timestamp will be the value of the System Timestamp at which the Fast Strobe output changed state. Triggers of this type are characterized by a Trigger Type Code of 0x55.
- If the trigger decision is reporting a trigger caused solely by an auxiliary detector input, then the Event Timestamp will be the value of the System Timestamp at which the change of state of the auxiliary detector trigger was sensed. Triggers of this type are characterized by a Trigger Type Code of 0x5A.
- If the trigger decision is reporting a trigger generated by a combination of inputs from multiple sources (e.g., an energy sum or a pattern trigger), then the Event Timestamp will be the lowest value (earliest) timestamp of all data included in the trigger decision. Triggers of this type are characterized by a Trigger Type Code of 0xA5.

7.3.1.2 DGS/DFMA-Specific Details

Dependent upon the type of trigger that is satisfied, the value of the Event Timestamp sent is resolved in one of two ways:

- If the trigger decision is reporting a trigger based upon SERDES information from the digitizers, then the Event Timestamp will be the value of the System Timestamp at which the enabled trigger algorithm (one of eight) made the decision; normally this is within 200ns of the receipt of the SERDES data. The Trigger Type Code shall encode which trigger algorithm was the cause of the decision (a number from 0x01 – 0x08).
    - Trigger Type Codes of 0x1-0x5 are indicative of triggers based upon conditions within the local detector.
    - A Trigger Type Code of 0x6 indicates a re-propagated remote trigger that was received through link L.
    - A Trigger Type Code of 0x7 indicates a re-propagated remote trigger that was received through link R.
    - A Trigger Type Code of 0x8 indicates a re-propagated remote trigger that was received through link U.
- Triggers caused by external inputs (e.g. NIM) shall report the System Timestamp at the time the edge in the front panel input was sensed. The Trigger Type Code shall in these cases be 0x00.

7.3.2 Broadcast versus specific trigger decisions

Additional, secondary trigger information may be sent in the auxiliary Front End Selection byte of the Trigger Decision command. The typical value of this byte will be zero, in which case it is expected that all front ends will respond (broadcast trigger). However, the master trigger may set this byte to a non-zero value. If the Front End Selection byte is non-zero, then only the front end whose Crystal ID is equal to the value of the Front End Selection byte may respond[2]. This allows the trigger to selectively trigger only one front end for a given trigger condition, allowing for the future possibility of special pattern triggers. It also may prove useful for system diagnostics. If some odd trigger condition requires a fixed set of front ends to respond, this will be handled by issuing multiple Trigger Decisions targeted to each of the selected front ends, using multiple command frames.

As the system develops, this functionality may also propagate into the TTCS itself, such that lower level trigger modules sense the value of the Front End Selection byte and block trigger decisions that don't involve their section(s) of the detector. This may be necessary if auxiliary detector front ends don't have the processing power to discriminate whether a trigger is meant for them or not.

[2] Note that this was the ***plan***, but to the best of the author's knowledge GRETINA digitizers don't work this way and instead simply ignore the Front End Selection byte. DGS/DFMA digitizers also ignore the Front End Selection byte.

7.3.3 Multiple trigger decisions within the same 2 microsecond period

The TTCS will, every 2 microseconds, determine if there are any triggers to be issued. The architecture of the Master Trigger allows for up to eight unique algorithms to be in play at any time. To accommodate this possibility, the TTCS implements a two-stage buffering system. Each enabled trigger algorithm (up to 8 are supported) implements a FIFO buffer in which trigger decisions are temporarily buffered. A trigger collection state machine collects up to eight triggers, *one per enabled algorithm,* in each two microsecond period. The first trigger in the collection buffer will be issued in the first command frame; the second trigger will be issued in the immediately following frame, and so on, until up to eight triggers have been issued. Under no circumstances will multiple triggers from the same algorithm be issued within a given 2usec period. The double buffer allows each individual algorithm to operate faster than 2usec; the limit is the time required to store a decision in the individual algorithm's FIFO (approximately 120nsec).

The buffers associated with each algorithm are not regularly cleared. If additional trigger conditions occur, they will pile up in the buffer and the next trigger available from each of the eight algorithms will be issued in the next two microsecond period. If, in any two microsecond period, less than eight trigger decisions are available to report, the unused Trigger Decision command frames will be replaced by null frames.

7.3.4 Trigger Decision selective propagation rules (DGS/DFMA only)

Each Master Trigger shall reserve frames 8, 9, and 10 for trigger messages from remote Masters connected to link L, R, and U respectively. Each Master will implement a "trigger algorithm" that collects triggers commands from frames 3 through 10 from each link and redirects them to the reserved trigger frames. By design, up to one external trigger command from each external trigger may propagate the digitizers every 2us. To control which external trigger types are allowed to propagate through the local trigger system, an array of control bit will be provided for each of the trigger algorithms that enables or disables the collection of triggers from each trigger frame (3 through 10) received from the remote Master Trigger. Each of the "external" trigger algorithms may also be completely disabled or enabled by another control bit.

Trigger decisions shall not be echoed back to the sender, as shown in the diagram below:

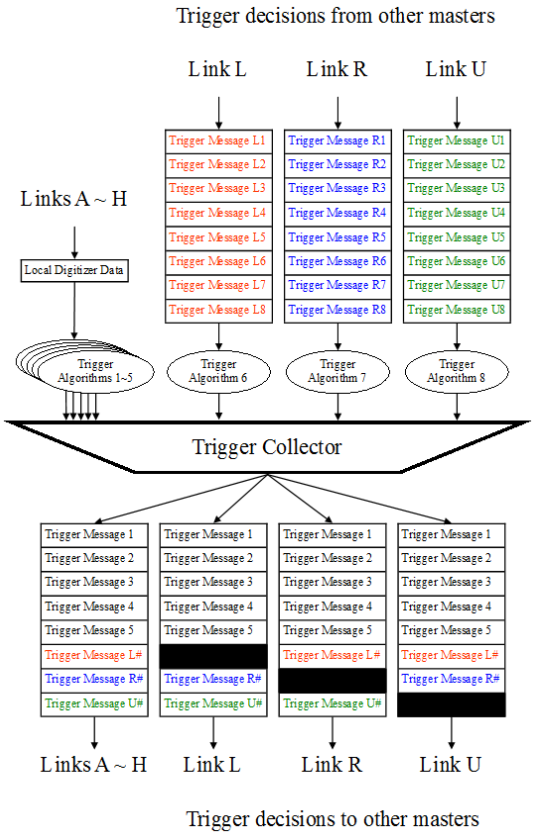

Figure 7: Flow chart of trigger decision propagation.

7.4 Frame 11 – Spare

Frame 11 is reserved for future use and will always contain the null command frame.

Word	Bits 16..1
1	0xAAAA
2	0xAAAA
3	0xAAAA
4	0xAAAA
5	0x0000

Table 10: Frame 11's payload.

7.5 Frame 12 - Internal Trigger Command

The Router Command Frame issued in Frame #12 normally is sent as a Null frame, but under specific conditions the Master may send a non-null frame in order to cause synchronous resets of the various diagnostic counters and FIFOs in the rest of the trigger modules in its hierarchical system. The Router is required to strip this frame from the data stream and replace it by a null frame so that any digitizer modules do not 'see' this command. The existence of a test module that generates digitizer-like data for testing, the Data Generator, is assumed. One trigger module has been re-purposed as a Data Generator in the ANL test stand. Digitizers may assume that Frame 12 will be a Null Frame.

Routers shall internally process Frame 12 data sent by Master Triggers but shall always send a Null Frame out links A-H. To allow for the connection of Data Generators or other test modules, the Router shall allow the unprocessed Frame 12 data to be driven out links R and U. The data sent by a Router out link L, by definition, is a unique experiment-specific Router-to-Master format that is separately documented.

When used for internal trigger command functions the internal structure of the frame is as given in Table 11.

Word	Bits 16..1
1	Command Byte
2	Router Counter Resets Bitmask
3	Router FIFO Resets Bitmask
4	Data Generator Resets Bitmask
5	0x0000

Table 11 – Structure of the Internal Trigger command as seen by the Router

7.5.1 Internal Trigger Command Details

Frame #12 is defined for internal trigger communication, specifically from the Master to Routers and to the Data Generator module. A register within the Master Trigger is programmed with a timestamp value. When armed by writing to another VME register, the System Timestamp is continuously compared against the timestamp value in the register; when a match occurs, exactly one non-null Frame #12 is sent. The Routers receive and respond to Frame #12 commands but strip the contents of Frame #12 out so that any digitizers connected to SERDES links ‘A’-‘H’ see only a Null frame. Links ‘R’ and ‘U’ of the Router, however, shall pass Frame #12 out unaltered so that a Data Generator module (whose link ‘L’ is connected to link ‘R’ or link ‘U’ of the Router – see section 4.2.1) can respond to Frame #12 commands.

When the frame is issued, the values in words #1 - #4 contain bit-mapped control values that are used by the Router and Data Generator to clear various counters and diagnostic FIFOs. Since the command is issued synchronously with a known timestamp value, this causes the FIFOs to sample all starting at the same moment in time, resulting in a system-wide “snapshot” of trigger activity. The first word of Frame #12 is, technically, a Command Byte Value of 0x00 with a

command argument of 0x01. While further refinement of the command is unlikely, expansion to new meaning of the following data words would be possible by modifying the first word.

7.5.2 Router Response to the Internal Trigger Command Frame

The Router Counter Resets bitmask affects the diagnostic counters of the Router. Bits 0:7 will, if set, cause the counters found at addresses 0x12C, 0x130,…,0x148, respectively, to reset to zero. The counters then count normally after being reset. Bits 15:8 of the Router Counter Resets value are currently unused. The Router Counter Resets value comes from a register in the Master Trigger. The Router FIFO Resets bitmask affects the diagnostic FIFOs of the Router. Bits 0:7 will, if set, cause the channel-specific FIFOs found at addresses 0x180, 0x184,…,0x19C to empty. Similarly, bits 8:15 will if set cause the board-wide "monitor" FIFOs found at addresses 0x160, 0x164,…,0x17C to empty. All FIFOs will capture normally immediately after the synchronous reset. The Router FIFO Resets value comes from a register in the Master Trigger.

7.5.3 Data Generator Response to the Internal Trigger Command Frame

The Data Generator Resets value uses only bits 3:0. The bits have the following functionality:

- Bit 0, if set, resets the event generation state machine of the Data Generator, resetting the pattern of events to the beginning. Bit 0 also resets the output state machines that emulate digitizer functions.
- Bit 1, if set, forces a clear of all diagnostic counters in the Data Generator.
- Bit 2, if set, forces a clear of all channel diagnostic FIFOs in the Data Generator.
- Bit 3, if set, forces a clear of all board-wide ("monitor") diagnostic FIFOs in the Data Generator.

The Data Generator Resets value comes from a register in the Master Trigger. The Data Generator shall not respond to Router commands in Frame #12, and Routers shall not respond to any Data Generator values sent in Frame #12.[3] The Master Trigger's running trigger counters may be reset during Frame 12 as might any Channel or Monitor FIFOs. Control of which Master Trigger features are reset during Frame 12 is controlled by two registers within the Master Trigger itself.

7.6 Frame 13 – Demand Front End Slow Data Command (GRETINA only)

In the GRETINA system, digitizers are assumed to be sending a mix of "fast" data (e.g. discriminator bits) and "slow" data (e.g. energy values), allowing for a mix of triggers based upon different information. In DGS and DFMA there is no "slow" data defined. The purpose of Frame #13 is to synchronize such "slow" data throughout the system. While the Master Trigger for DGS/DFMA will retain the GRETINA format of Frame 13 for backwards compatibility, there is no expectation that the digitizers of DGS/DFMA will respond to this frame in any meaningful way.

[3] While this is the intent, the GRETINA Data Generator firmware may, in fact, also respond to Router commands to clear FIFOs and/or counters too.

7.6.1 Demand Front End Slow Data command

Word	Bits 16..9	Bits 8..1
1	0x40 (hex)	0xFB
2	0xA5A5	
3	0x5A5A	
4	0xA5A5	
5	0xA5A5	

Table 12: Format of Demand Front End Slow Data command.

The Trigger Data link, in GRETINA, is assumed to be continuously transmitting "fast" data corresponding to discriminator outputs. However, energy sums and segment hit patterns are only available at slower rates. The Demand Front End Slow Data command, like the Sync command, is *always* issued at a regular rate without interruption. In response to this command, the front ends all issue a Trigger Data frame with segment and energy information. It is assumed that a frame is always available even if no segments were hit or if the measured energy is below threshold. This results in the orderly and regular transmission of energy information every two microseconds and allows sufficient time for all this data to propagate to the top of the trigger hierarchy before the next set of data is transmitted.

The 0x40/0xFB Command Byte is simply chosen to be easily recognizable, but has no specific meaning. This command is specific and unique to digitizers in the GRETINA system. Digitizers used in DGS or other detectors ignore this command as the Trigger Data link format of DGS is all "fast" data with no "slow" data to control.

7.6.2 Frame 14 - Internal Trigger Command (DGS/DFMA only)

Frame #14 works in the same general fashion as Frame #12, although the intended target of Frame #14 commands is different. Frame #14 is reserved for communicating with Digitizer Tester boards in the test stand, or for synchronizing operations with a MyRIAD board. As such, the format for Frame #14 consists of a couple words defined for use with the Digitizer Tester plus some reserved space for future expansion. GRETINA trigger boards do not implement this functionality and only send Null frames in frame #14.

The Router Command Frame issued in Frame #14 normally is sent as a Null frame, but under specific conditions the Master may send a non-null frame in order to cause synchronous resets of various diagnostic counters and FIFOs in the rest of the trigger modules in a hierarchical system. The Router masks any non-null frame sent in Frame #14 and always replaces it by a null frame when retransmitted to the digitizers so that the digitizers are unaware of any commands issued in this frame.

Word	Bits 16..1
1	0xAAAA
2	0xAAAA
3	0xAAAA
4	0xAAAA
5	0x0000

Table 13: Frame #14 as sent by Routers to Digitizer modules.

7.6.3 Internal Trigger Command (command byte not equal to 0xAA)

Word	Bits 16..1	
1	Command Byte	0x00
2	Timestamp Bitmask (matches TS bits 25:10)	
3	Pulse Count	Pulse Delay
4	Reserved	
5	0x0000	

Table 14: Format of Internal Trigger Communication Frame #14

The Command Byte of frame #14 may take on multiple values depending upon the desired action within the Digitizer Tester. The Tester implements a waveform buffer of DAC samples that may be “played” upon command, generating useful test waveforms for digitizers.

The following Command Byte values are defined:

- 0x00: Stop sending pulses, go quiet, shut up!
- 0x01 : Issue single pulse NOW.
- 0x02: Enter Loop mode and begin issuing signals NOW.
- 0x03: Cease Loop mode and stop issuing signals at end of next set of buffers.
- 0x04: Begin issuing pulses tied to timestamp. This mode uses the Timestamp, Pulse Count and Delay parameters as follows:
    - Each time the selected bit of the Timestamp transitions 0->1, issue a series of <Pulse Count> pulses, delayed from each other by <Delay> counts.
    - The units of Delay are in units of 100s of nsec, and it is the time from the end of pulse 'n' to the beginning of pulse 'n+1'.
- 0x05 – 0x0F are reserved.
- 0xAA is sent for the null case (no command).

The Reserved word is reserved for MyRIAD use and its value is at present undefined. The word of 0x0000 at the end may also be used for MyRIAD control at some future time.

7.7 Frame 15 – GRETINA Front End Asynchronous Command

Front End Asynchronous commands are sent only in response to a request from the slow control and monitoring system. The vast majority of the time, the time-slice allocated to this command will be filled with a null command. The format of Front End Asynchronous commands is open, although specific suggestions for commands that could be implemented herein are given below. The Front End Asynchronous command is implemented using a 256-word deep, 16-bit wide FIFO that may be written to from VME. Slow control software is free to write into this FIFO whatever commands desired and the interpretation of these commands is left to the Digitizer.

It is the responsibility of the slow control software to insure that the data written to the Asynchronous Command FIFO does not accidentally emulate any other command in the system. To help insure this it is recommended that the upper byte of the data written in the word that will become the first word of the command sent in frame #15 be constrained to the values 0x04, 0x08, 0x10 or 0x18. Should further expansion be necessary at some future time it is recommended that the new command values be taken from the range 0xB0 – 0xEF. The trigger samples the Empty state of the Asynchronous Command FIFO every system cycle and extracts five words from the FIFO to fill the frame if data is available.

This command is specific to and reserved for the GRETINA version of the digitizer. The DGS digitizer firmware ignores this frame and control software for other experiments is expected to not attempt to use this frame.

7.7.1 Suggested Format and Operation of Calibration Inject Command (command byte = 0x04 or 0x08)

The following is a suggested implementation of the Calibration Inject asynchronous command. Adherence to this section is not required.

When this command is sent, front end units shall respond according to the value in the Addressing Control byte:

- If the Addressing Control byte is 0x00, *all* front ends shall perform a calibration inject cycle and the Selection Bitmask values shall be ignored.
- If the Addressing Control byte is nonzero, the following eight bytes of data shall be interpreted as a bit mask selecting any arbitrary combination of up to 64 front end units to perform the calibration cycle.
  - To allow for further system expansion, the value of the Addressing Control byte may be used to select one of *n* groups of up to 64 front ends.
  - It is recommended that the bit number associated with each front end be consistent with its Crystal ID value (e.g., bit 6 of bits 63..0 is associated with crystal #6).

The trigger shall not implement any timer or other method to separately process events generated by a Calibration Inject request. The trigger shall require that events presented upon the Trigger Data link in response to a Calibration Inject are indistinguishable from "normal" events. It should be assumed by the reader that the TTCS is aware that a calibration inject cycle has been requested and that the trigger may override normal trigger acceptance settings in order to insure that a Trigger Decision command will be issued when the data associated with the Calibration Inject sequence is delivered.

Word	Bits 16..9	Bits 8..1
1	0x04 (hex)	Addressing Control
2	Selection Bitmask[63..57]	Selection Bitmask[56..48]
3	Selection Bitmask[47..40]	Selection Bitmask[39..32]
4	Selection Bitmask[31..24]	Selection Bitmask[23..16]
5	Selection Bitmask[15..8]	Selection Bitmask[7..0]

Table 15: Format of Front End Calibration command.

7.7.2 Suggested Format and Operation of Latch Status command (command byte = 0x08)

The following is a suggested implementation of the Latch Status asynchronous command. Adherence to this section is not required.

The Latch Status command demands that all front end units save a status record for readout by the slow control and monitoring system. If implemented, any error reported by any front end via the Trigger Input Data link should force this command to be issued to all front ends.

Word	Bits 16..9	Bits 8..1
1	0x08 (hex)	Status Control Byte
2	Auxiliary Information Word 3	
3	Auxiliary Information Word 2	
4	Auxiliary Information Word 1	
5	Auxiliary Information Word 0	

Table 16: Format of Latch Status command.

7.7.3 Suggested Format and Operation of Front End Reset command (command byte = 0x10)

The following is a suggested implementation of the Front End Reset asynchronous command. Adherence to this section is not required.

The Front End Reset command demands that the selected front end digitizers perform a complete reset. The selection mechanism is identical to that used described above for the Calibration Inject command. The TTCS may perform internal recognition of this command to the extent where it internally masks the Trigger Data input stream from any or all front ends selected to be reset until the slow control system informs the trigger that the inputs are again valid. Once the slow control system informs the trigger that the inputs are again valid, the input masks will be removed synchronous with the issuance of the next Sync command.

Word	Bits 16..9	Bits 8..1
1	0x10 (hex)	Addressing Control
2	Selection Bitmask[63..57]	Selection Bitmask[56..48]
3	Selection Bitmask[47..40]	Selection Bitmask[39..32]
4	Selection Bitmask[31..24]	Selection Bitmask[23..16]
5	Selection Bitmask[15..8]	Selection Bitmask[7..0]

Table 17: Format of Front End Reset command.

7.7.4 Suggested Format and Operation of Front End Links-only Reset command (command byte = 0x)

The following is a suggested implementation of the Front End Reset asynchronous command. Adherence to this section is not required.

The Front End Links-only Reset command demands that the selected front end digitizers perform a partial reset, limited only to their serial Trigger Data output links. From the standpoint of the TTCS, this command is handled identically to command 0x10 (Front End Reset). The internal masks will be set and held until released by the slow control system.

Word	Bits 16..9	Bits 8..1
1	0x18 (hex)	Addressing Control
2	Selection Bitmask[63..57]	Selection Bitmask[56..48]
3	Selection Bitmask[47..40]	Selection Bitmask[39..32]
4	Selection Bitmask[31..24]	Selection Bitmask[23..16]
5	Selection Bitmask[15..8]	Selection Bitmask[7..0]

Table 18: Format of Front End Links Reset command.

7.7.5 Suggested Format and Operation of External Discriminator Request (command byte = 0x22)

The following is a suggested implementation of the External Discriminator Request command. Adherence to this section is not required.

The External Discriminator Request command provides a mechanism by which a single write to the Master Trigger module can initiate a discriminator firing synchronously across multiple digitizer channels. The Addressing Control field is used to select the channels of the digitizer that are to respond. As the digitizer has 10 channels a simple bit-map cannot be used, so instead a 10-bit selection mask is provided in word 2. Selection of which digitizers are to respond is provided through the User Package Data AND mask plus the User Package Data OR mask. The User Package data value written into each digitizer by the user is first bit-by-bit ANDed with the AND mask, and the resulting value is then bit-by-bit ORed with the OR mask. If the resulting value after both operations is non-zero, the digitizer will respond to the command. An OR mask of 0xFFF results in a broadcast that all digitizers will honor.

The ‘SL’ (**S**et **L**atch), ‘CL’ (**C**lear **L**atch), ‘EL’ (**E**nable **L**atch) and ‘DL’ (**D**isable **L**atch) bits are provided to allow for a latched mode of operation. The default mode of operation is non-latched, where the External Discriminator bit to a selected digitizer is asserted for one clock cycle at the end of the External Discriminator Request frame. Upon receipt of any command with the ‘EL’ bit set, each selected digitizer will enter a latched mode controlled by the ‘SL’ and ‘DL’ bits. In the latched mode, each selected digitizer will set or clear the latch based upon the ‘SL’ and ‘DL’ bits (if both are clear or both are set, the latch status will not change). The latched mode of operation is intended to work with the “AND” mode of the external discriminator logic of the DGS digitizer so that the trigger may simultaneously gate internal discriminators on and off. Once in the latched mode a digitizer stays in the latched mode until a command with the ‘DL’ bit is received, after which the digitizer returns to non-latched operation.

Word	Bits 16..9							Bits 8..1
1	0x22 (hex)							0x00
2	EL	DL						Channel select bitmask[10:1]
3	SL	CL			User Package Data AND mask[12:1]			
4					User Package Data OR mask[12:1]			
5	0x0000							

Table 19: Format of External Discriminator Request.

7.8 Frame 16 – DGS Synchronous System Capture Command

The vast majority of the time, the time-slice allocated to this command will be filled with a null command. The purpose is to provide a mechanism by which event rates and detector firing rates may be accurately and repeatedly measured. This command is supported by the version of digitizer firmware used at DGS but other systems may adopt it.

7.8.1 Synchronous System Capture Implementation

A write to a register within the Master Trigger causes the issuance of the Synchronous System Capture Command. The format of the Synchronous System Capture Command is given in Table 20. When no command is being issued, the Command Byte is 0xAA; any other value indicates a command is in progress. The Argument Byte is not used and hardcoded to 0x00. The Timestamp, Capture Length and FIFO Capture Delay values sent with the command are all sourced from registers within the Master Trigger.

When the command is issued, it shall be received and decoded by any device below the Master in the hierarchy (Router, Data Generator, Digitizer or Digitizer Tester). MγRIADs and other Master Triggers co-equal to the Master issuing the command ***do not*** respond ***unless*** they have been programmed to by setting appropriate bits in their respective command propagation control registers – this is identical logic to propagation of Trigger Decision messages. Each device that does respond to Frame #16 commands shall do so by zeroing all of its system event rate counters (digitizer: counts of discriminator firings per channel and count of events passed to FIFO; trigger modules: counts of trigger types issued and counts of triggers vetoed). These counters are then enabled until the capture time elapses. When the capture time elapses, the counters stop counting and a bit is set in a status register indicating 'capture complete'. The system software may then take as long as needed to collect the status data as no more system-wide captures will occur unless software asks for it again.

Word	Bits 16..9	Bits 8..1
1	Any value not 0xAA	0x00
2	Timestamp(15:0)	
3	Capture Length	
4	FIFO Capture Delay	
5	0x0000	

Table 20: Format of the Synchronous system capture front end command.

The 32-bit Timestamp value sent is compared against bits 31:0 of the system timestamp in each module to initiate collection. The Capture Length value defines the number of 16-bit rollovers of the timestamp (period of 65.536us), that the device shall collect event statistics in counters before halting counters/FIFOs and setting the 'capture complete' status bit. This allows for a maximum collection time of (65,536 * 65.536us), or approximately 4.3 seconds. A Capture Length of 15,258 provides a collection time of 0.99995 second. Within the firmware, collection starts when the device timestamp is equal to the 32-bit Timestamp value within the command. The

Capture Length is added to the upper 16 bits of the 32-bit Timestamp value within the command and collection persists until the device timestamp is equal to the result of that addition.

A device receiving this command may have diagnostic FIFO buffers to capture ADC samples or SERDES messages in addition to rate counters. Any FIFOs controlled by the Synchronous System Capture operation shall reset immediately upon the match of the timestamp; logic that controls the FIFOs shall then wait for an amount of time equal to the FIFO Capture Delay value, in shifted timestamp count units identical to those of the Capture Length, before enabling the FIFOs to start filling. This allows the data collection window for diagnostic FIFOs to be offset relative to the start time at which diagnostic *counters* began counting in a capture operation, as such FIFOs are unlikely to be deep enough to capture milliseconds' worth of data. For instance, one could set the Capture Length to 15,258 to collect counts for almost exactly one second but set the FIFO Capture Delay equal to 12,250 so that the FIFOs start collecting at 0.802 seconds after the start of the capture time.

In the specific case of the Router, any FIFOs that are controlled by Frame #12 commands (see section 7.5) are ***not*** required to respond to this command. The Router may allocate counters and FIFOs either to Frame #12 or Frame #16, but there is never a requirement that any counter or FIFO must respond to both Frames.

The Master Trigger *shall* respond to commands issued in Frame 16. A set of sixteen counters shall be implemented that reset and capture counts of triggers during the same capture interval as specified for the front ends. The first eight of these counters shall capture the number of triggers of each trigger type that were issued to the front ends during the capture interval. The second set of counters shall count the number of triggers that *might* have been issued, but were blocked from doing so by a digitizer throttle request or an externally applied Trigger Veto input. The sum of the two counters (issued and non-issued), per trigger algorithm, shall be the total number of times the given algorithm was satisfied during the interval; the ratio of the two is the "dead time" percentage. The counters implemented for Frame 16 shall be unique and separate from the running counters described for Frame 12 use in section 7.5.1 above.

7.9 Frame 17 - Auxiliary Detector Commands

These are generic commands whose format is indeterminate, implemented in an identical fashion to the Front End Asynchronous Command of frame #15. This command implements its own unique Auxiliary Command FIFO of the same size and format as the Asynchronous Command FIFO, and a different bit in the VME control register is used to enable the transmission of these values. These are reserved for use with non-digitizer front end devices (other than the MγRIAD) to provide a command distribution mechanism. For the MγRIAD, use Frame #14.

7.10 Frames 18 & 19 - Null command

The Null command is a placeholder that shall cause no activity in any trigger module or front end device. It is transmitted as a placeholder in any command frame where no activity is required (e.g. Trigger Decision frames when there is no trigger, frames reserved for slow control activity where none is currently called for, etc.). Since this is expected to occur most of the time, the best use of the Null frame is to send a pleasant pattern that's easily recognized on the oscilloscope that also happens to assist with line DC balance. The command byte of 0xAA is the preferred value used by the TTCS for all Null commands.

Word	Bits 16..1
1	0xAAAA
2	0xAAAA
3	0xAAAA
4	0xAAAA
5	0x0000

Table 21: Frame 18 & 19's payload.

7.11 Frame 20 - End-of-Cycle

7.11.1 End-of-Cycle command (command byte = 0xFF)

The End-of-Cycle command is transmitted only at the end of the trigger cycle and is used to establish a frame boundary marker. Essentially, it is a special form of the Null command. The sequence of values is chosen to make this frame easily distinguishable by the human reader in data dumps.

Word	Bits 16..9	Bits 8..1
1	0xFF	0xFF
2	0x0000	
3	0xFFFF	
4	0x0000	
5	0x5555	

Table 22: Format of End-of-Cycle command.

8. INITIALIZATION CONSIDERATIONS

At system startup the TTCS shall initialize itself to a special state wherein the timing cycle is modified. During this initialization phase command frames 1 and 20 will be driven normally but all other command frames will be forced to Null commands. The initialization phase shall persist until the slow control system releases the trigger from that state. Normal operation will then begin with the next full trigger cycle, beginning with the Sync command of frame #1. A reset of the trigger will cause this initialization to be repeated.

Note: The "initialization mode" is in the process of being deprecated. At some point in the near future both the initialization mode and any vestigial remains of the "Debug Command" (frame #2) shall be completely removed.

8.1 What if the TTCS has to be reset?

Generally, reset of the Trigger system should never be required. If, due to some extremely odd case, this is required, the simplest methodology is to power-cycle the crate, re-initialize the links and resume operation. The only possible condition envisioned that could require a reset is some case in which a large burst of triggers from some source overflows a FIFO in the trigger path. Individual FIFOs associated with the trigger algorithms are reset by simply turning that algorithm off and then on again.