MyRIAD User Manual

-- PRELIMINARY --

March 19, 2015
Version 1.2

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TABLE OF CONTENTS

1   GENERAL INFORMATION

The MyRIAD (Multipurpose gamma Ray Interface to Auxiliary Detectors) module provides a general-purpose interface to allow other detector systems that work in concert with the digital data acquisition (DAQ) sytems of Digital Gammasphere[1] (DGS) and GRETINA[2] to receive the timestamp and triggering information from the triggering system of those systems and use that for synchronization within the data acquisition system of an auxiliary detector used in concert with these large detector arrays. Additionally the MyRIAD may be used to transmit time-stamped trigger messages from the auxiliary detector to the main system so that the main system may filter its event readout based upon the presence or absence of a local trigger in the auxiliary detector. Finally, the MyRIAD provides signal interface capabilities designed to allow legacy CAMAC-based detector DAQ systems to be directly controlled and interfaced by the DAQ system of DGS or GRETINA.

1.1   Description of Component & How It Fits Into the System

A MyRIAD sits in the VME crate used for data acquisition in an experiment external to DGS or GRETINA. A CAT5 cable or optical fiber runs from the master trigger module to the MyRIAD providing bi-directional data communication and clock synchronization between the two systems. External signals from the local detector logic indicative of local triggers are connected to front panel inputs of the MyRIAD. Logic within the MyRIAD latches the master trigger's timestamp when local triggers occur, allowing inclusion of the DGS/GRETINA timestamp into the readout of the external detector data stream for later merging of events by timestamp.

The MyRIAD may also function as a gating logic module, receiving trigger messages from master trigger and using those messages to gate local triggers within the external experiment. Similarly, the MyRIAD may simply receive triggers from the external experiment and pass them over the link so that DGS/GRETINA triggering may be gated by the external experiment. Figure 1 shows the overall connection scheme at Digital Gammasphere, where the MyRIAD is shown interfacing the Auxiliary Detector system to the Master Trigger of Digital Gammasphere.

In Figure 1, the DGS data acquisition system master trigger is considered the "system monarch" as it has two subservient timestamp domains. The clock and timestamp from the DGS master trigger is sent to the master trigger in the DSSD (Dual-sided Silicon Strip Detector) system, so that acquisition in these two systems are synchronized. The MyRIAD in the Auxiliary Detector also is synchronized to the clock and timestamp from the DGS master trigger, so that events in all three systems have correlated timestamps. The bidirectional nature of the SerDes links between the "monarch" and its two subservient systems allows the "monarch" to collect and re-propagate trigger messages from either or both outside systems into its local domain. This allows DGS to trigger and collect events based upon triggers local to itself, triggers based upon conditions in the outside systems, or combinations thereof. This allows for complex event selection to reduce event rate in high intensity beams.
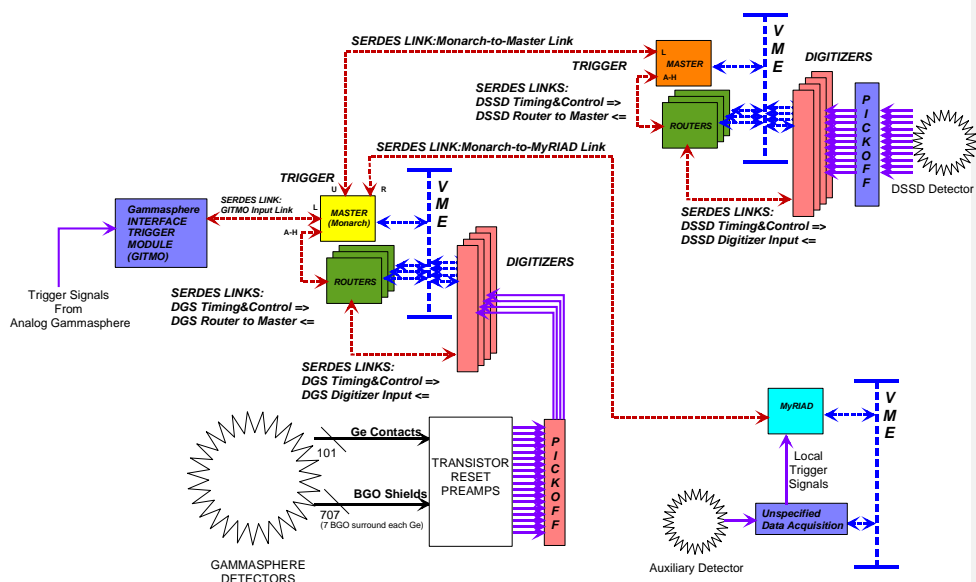
Figure 1 – Overall connectivity between detector systems at Digital Gammasphere

The GRETINA system uses the same trigger and digitizer module hardware, but with different firmware specific to that detector's geometry. In Figure 1, the Master Trigger module of DGS is the root source of the system sampling clock and timestamp. Through fixed-latency 1Gbps serial link hardware (hereafter referred to as SerDes, an acronym for Serializer/Deserializer), a continuous stream of trigger, timestamp synchronization and command information is distributed throughout Digital Gammasphere from the Master Trigger through Router Trigger modules to the Digitizer modules, resulting in all digitizer channels synchronously sampling. A second, identically structured DAQ system near DGS named DFMA (Digital Fragment Mass Analyzer) instruments a dual-sided silicon strip (DSSD) detector along with other types of detector elements. The DFMA system has its own Master Trigger, allowing it to run independently of DGS as needed; however, the Master Trigger of DFMA may be set to receive and re-propagate the clock from the DGS Master, resulting in both digital data acquisition systems sampling in lockstep. As the original 'analog' (non-sampling, charge-injection ADC) DAQ of Gammasphere is still in existence, an option has been provided to allow the DGS Master access to signals from that system through the GITMO (Gammasphere Interface Trigger Module) for comparative performance measurements.

In the Auxiliary Detector system of Figure 1, the MyRIAD has a bi-directional SerDes connection to the Digital Gammasphere master trigger. This allows the MyRIAD to implement a timestamp counter identical to those in all the digitizer modules in DGS and DFMA, so that events in the Auxiliary Detector are tagged with timestamps that are synchronous to those in the other systems. When the Auxiliary Detector reads out its data the propagated DGS timestamp of those events is included, allowing direct correlation of Auxiliry Detector events to those in DGS

and DFMA. In the opposite direction, local trigger signals connected to the front panel of the MyRIAD in the Auxiliary Detector crate cause SerDes messages to be transmitted to the DGS master trigger, whose firmware may then attach a timestamp to those messages and cause correlated DGS data to be read out based upon trigger conditions in the Auxiliary detector.

A specific and detailed protocol for the SerDes communication between the various modules has been developed. To allow other detector systems to leverage the power of this timestamped, SerDes-based triggering scheme the MyRIAD has been developed to implement full protocol and extend it to other detectors. The simultaneous use of auxiliary detectors to augment the research capabilities of Gammasphere is a well-developed activity within the low-energy physics community that has been in play from 1996[3] through the present day. The rollout of the new DAQ system of Gammasphere (DGS), begun in 2012, including the development of the MyRIAD, allows this tradition of multi-detector operation to continue and allows for more complex cross-detector triggering schemes than were possible before.

1.2   List of Functional Requirements

The overall requirements of the MyRIAD are as follows:

- SerDes interface compatible with Trigger Timing and Control Link specification[4] (i.e. receive commands like a Router)

- SerDes interface capable of sending triggering information to Master Trigger

- VME 6U module capable of operation in standard or VME64x crate, using either A32/D32 or A24/D16 transaction types

    o Have +3.3V power wiring compatible with either kind of crate – standard VME does not supply +3.3V but VME64x does

    o Have appropriate addressing mechanisms for standard VME (DIPswitch) or VME64x (geographic addressing)

- Provide multiple front panel inputs and outputs in both NIM and differential ECL for interface to a variety of detector logic including other VME modules, NIM and CAMAC

- Provide a registered or buffered mechanism of saving timestamps of events to support either single-event or multi-event data acquisition models in the external detector

- Implement sufficient logic capability to perform windowed timestamp matching and trigger signal gating

Some auxiliary detector systems still implement CAMAC ADCs such as the FERA system. 'Analog' Gammasphere provided an interface for such modules to be integrated into the system by use of a custom module that mechanically combined a custom FERA-to-VXI input interface with a commercial (now obsolete and unavailable) VME-to-CAMAC branch highway controller. To accommodate this possibility, the MyRIAD implements sufficient ECL I/O to act as both a FERA readout controller and a FERA input buffer.

1.3   General VME information

The VME mode (A24/D16 or A32/D32) of the MyRIAD is selected by the version of firmware that is loaded into the its VME interface FPGA. The firmware normally loaded is the A24/D16 version that is compatible with all forms of VME crates. In this version, a DIP switch sets an eight-bit base module address that is compared with bits 23:16 of the VME address asserted by the crate controller. If the upper bits match the MyRIAD will respond to any address within the range 0xdd0000 through 0xddFFFC, where 'dd' is the value set by the DIP switches. Throughout this document reference will be made to register addresses within the MyRIAD. All such addresses shall be described as a four-digit hexadecimal number (i.e. from 0x0000 to 0xFFFC). These addresses should be interpreted by the reader as the lower 16 bits of the 24-bit address range that the MyRIAD has been set to respond to.

With appropriate firmware loaded into the VME interface FPGA the MyRIAD may operate in the A32/D32 mode. The MyRIAD is constructed using connectors compatible with "VME64x" backplanes and a resistive sensing circuit allows the VME interface FPGA to sense the presence or absence of pins specific to the VME64x connector. This allows the MyRIAD to sense whether the VME64x backplane's Geographic Address pins are available, and if so, to use them to set the base address of the board according to VME64x specifications.

The majority of control registers implemented by the firmware in the MyRIAD's FPGAs are readable and writable with the register reading back the last value written to it. All status registers are read-only; writes to status registers have no effect. A few control registers are "write only", used to generate internal timed pulses when 1s are written to certain bits.

1.4   Board Photo - front

Indicator LEDs. The 'V' LED blinks when the board is accessed via VME. The two 'P' LEDs are power status. The two 'F' LEDs indicate FPGA status. The four 'S' LEDs are general status.

The RJ-45 connector is NOT ETHERNET. This connector uses Cat5e cable for a copper connection to DGS/GRETINA trigger modules only. The LEDs of this connector indicate the state of the connection to the master trigger.

The JTAG connection provides direct access to the FPGAs using a Xilinx JTAG programming adapter.

The ECL CTL connector provides a mix of differential ECL inputs and outputs. The pinout is compatible with the control connector of a FERA interface but the usage of the signals is not fixed; firmware may define them as required.

Similarly the ECL I/O connector provides 16 differential ECL signals for general purpose use. The board provides assembly positions so that either ECL driver chips or ECL receiver chips may be installed. The default is 16 bits of receiver. 100 ohm termination resistors for each differential input are provided.

Eight NIM-level inputs and four NIM-level outputs are provided. Note that the connections are grouped into two sets of four inputs and two sets of two outputs indicated by the letters I (for Input) and O (for output). The usage of all 12 signals is defined by firmware. Normally Input 0 at top left is used as the "local system trigger input".

1.5   Board Photo – side
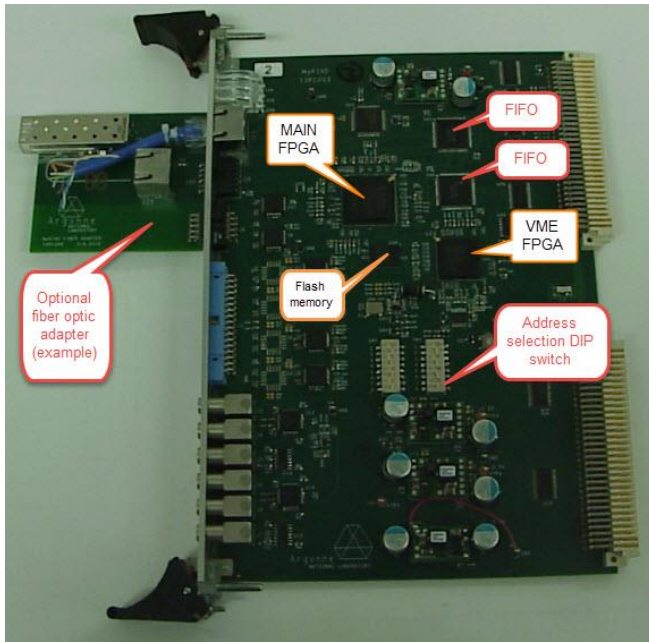
2   THEORY OF OPERATION AND OPERATING MODES

2.1   Basic Features & Operation (Including Block Diagram)

A block diagram of the MyRIAD is provided as Figure 2. The VME FPGA handles all the VME cycle decoding and manages firmware download into the Main FPGA. This logic is derived from firmware developed for the DGS trigger and digitizer boards. The Main FPGA is a moderate size Spartan-3 XC3S1000 FPGA. An external large FIFO is provided to handle the possibility of high event rates and/or the FERA readout option.
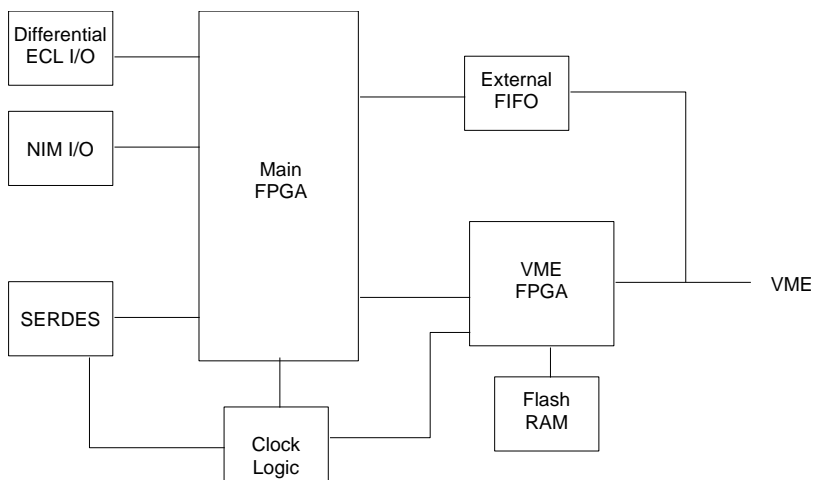
Figure 2 – MyRIAD logic block diagram

2.2   SerDes Data Path

The SerDes data path is bi-directional. Commands, triggers, clock and timestamp are received by the MyRIAD from the Digital Gammasphere Master Trigger. The MyRIAD reports on local trigger conditions read from the NIM and/or ECL inputs back to the Digital Gammasphere Master Trigger over the other half of the SerDes.

2.2.1   Connecting the MyRIAD to the master trigger

The MyRIAD implements a receiver state machine essentially identical to that of the router trigger or the digitizer. User software is required to first note that a physical SerDes link is present by interrogating the SerDes LOCK* signal via bit 10 of the HARDWARE_STATUS register located at address 0x0020. Once a physical link lock is achieved the reception state machine will attempt to lock onto the command stream from the master trigger but will be unable

to achieve a stable lock until the clock of the MyRIAD is phase- and frequency-locked to that of the master trigger.

To switch from the internal clock to use the SerDes clock, bit 15 of the SD_CONFIG (SerDes Configuration) register at address 0x0848 must be set. The reception state machine should then be able to reliably process the command stream. This may be verified by writing to bit 2 of the PULSED_CTRL register to clear the "RX machine lost lock" bit found as bit 14 of the HARDWARE_STATUS register, and verifying that the lost lock bit is not re-asserted.

2.2.2   Trigger communication

The MyRIAD monitors local triggers from its host detector system using either NIM input 0 (the default) or the differential ECL "FERA WSI" input (if selected by user software). A pulse no less than 100ns wide should be used. When the leading edge of the local trigger occurs, a trigger message is sent over the SerDes link from the MyRIAD to the master trigger module containing the timestamp (as latched by the MyRIAD) when the trigger occurred. Control registers within the master trigger then enable or disable re-propagation of the MyRIAD trigger into the master trigger's domain. If enabled, the trigger message from the MyRIAD is retransmitted to all digitizers of the DGS/GRETINA system. Any gamma events in the digitizers whose timestamps fit within the time window specified relative to the timestamp in the trigger message are then flagged for readout, allowing the MyRIAD to select gamma events in DGS/GRETINA based upon the local trigger of the auxiliary detector.

Triggers generated by DGS/GRETINA are also received by the MyRIAD over the SerDes link. A NIM output pulses each time a trigger message is received and may be used by local detector logic to form coincidences in the local detector; however this pulse will have significant and variable propagation delay because of the way the DGS/GRETINA triggering logic works.

Commented [JTA1]: Which one?

Commented [JTA2]: Latest firmware should reduce this to significant, but not variable.

2.2.3   Timestamp latching

At the same moment that the timestamp of the local trigger is latched by the MyRIAD for transmission to DGS/GRETINA, that same timestamp is latched and a message is written into the board-wide FIFO. If software for the MyRIAD's detector reads out the MyRIAD FIFO as part of every locally triggered event, the DGS/GRETINA timestamp is then added to the data for the remote detector allowing software matching of events across detectors by timestamp. The timestamp latch may also be used, but this entails the risk that another local trigger may occur during the time that the latch is being read out. Lockout logic within the MyRIAD ensures that the latch value is not corrupted by a trigger occurring during readout but it is possible to miss such triggers if more than one occurs during the readout time.

2.3. Control Path Descriptions

All control of the MyRIAD flows through the VME FPGA. At power up the VME FPGA loads firmware into the main FPGA from the on-board flash memory and all VME transactions are mediated by the VME FPGA. Reads of the external FIFO over VME are mapped to a specific address by the VME FPGA. All normal control of the MyRIAD is accomplished using register reads and writes over the VME bus.

The MyRIAD receives and processes all command frames from the master trigger module.   Future firmware updates will implement support of Auxiliary Detector and Synchronous System Capture commands from the master trigger. These updates will allow the MyRIAD to perform additional functions including synchronous event rate measurements at the same time such measurements are being made in DGS/GRETINA and assertion of control signals to the local detector at specific timestamps for coordination of control actions such as resets, calibration triggers, etc.

2.3   Coincidence Logic within the MyRIAD

A small state machine within the MyRIAD provides some basic coincidence logic for trigger gating. The logic begins operation when the trigger signal from the local detector arrives. Bits 0 and 1 of the GATING_REG register at address 0x0702 select what the "starting trigger" is. When bit 0 is set, the "starting trigger" is the signal applied to NIM input 0 (the local detector trigger). If bit 1 is set, the "starting trigger" is the receipt of a trigger message via the SerDes link from the DGS/GRETINA master trigger module. Once the "starting trigger" occurs, a delay interval defined by the value in Coincidence Delay Register (address 0x0710) multiplied by 20ns is enforced.

Once the Coincidence Delay time has elapsed, a second timing interval defined by the Coincidence Window Register (address 0x0712) begins. During this second interval, if a signal edge is applied to NIM input 1, a coincidence output signal pulse occurs on NIM output 3. If the second interval elapses without an edge on NIM input 1 the state machine returns to waiting for a "starting trigger".

3   DETAILED INTERFACE SPECIFICATIONS

3.1   Firmwae Maintenance

As in the other Digital Gammasphere modules, the program for the VME FPGA is held in a small PROM accessible only by JTAG. It is expected that the VME FPGA program will rarely change, but the JTAG connector is available at the front panel. This connector is compatible with the 'flying leads' option of Xilinx-compatible JTAG interfaces. The main FPGA program is held in flash memory that is accessible from VME. The main FPGA program is automatically put into the main FPGA by the VME FPGA at power-up. The user may, with appropriate software, download a new binary image file into the flash memory that will change the program of the main FPGA after a power cycle or reconfiguration request.

3.2   Internal Control Registers

Table 1 shows a summary list of the registers provided within the MyRIAD. The detailed description of each register follows in a separate section.

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Address	Register Mode	Register Name	Function
0x0000	R	board_id	Contains address and firmware information.
0x0004	RW	fifo_status	Contains FIFO status.
0x0020	R	hardware_status	Contains DCM status information
0x040C	W	pulsed_control	Write only (self clearing) register. Used for resets.
0x040E	RW	fifo_control	Controls FIFO operational modes.
0x0410	RW	Capture_time	Sets capture time when using FIFO to test SerDes
0x0600	R	code_revision	Holds the code revision of the board
0x0604	R	code_date	Reads back code date of compilation (mmdd)
0x0606	R	Code_year	Reads back year of code date (yyyy)
0x0700	R	NIM input status	Reads back current status of NIM inputs
0x0702	RW	Gating register	Controls usage of NIM signals to gate triggers
0x0704	R	ECL input status A	Reads back current status of ECL data inputs
0x0706	R	ECL input status B	Reads back current status of ECL control inputs
0x0708	R	LATCHED_TIMESTAMP_A	Bits 47:32 of latched timestamp
0x070A	R	LATCHED_TIMESTAMP_B	Bits 31:16 of latched timestamp
0x070C	R	LATCHED_TIMESTAMP_C	Bits 15:0 of latched timestamp
0x070E	RW	SerDes_COMMAND_FORMAT	Selects SerDes command format (DGS/GRETINA)
0x0710	R	Coincidence window delay	How long to wait after local trigger for match
0x0712	R	coincidence window width	How wide a gate for a GS trig match
0x0714	R	LIVE_TIMESTAMP_A	Bits 47:32 of running timestamp
0x0716	R	LIVE_TIMESTAMP_B	Bits 31:16 of running timestamp
0x0718	R	LIVE_TIMESTAMP_C	Bits 15:0 of running timestamp
0x071A	RW	TIMESTAMP_ERROR_CTRL	Allows reset of timestamp error counter
0x071E	R	TIMESTAMP_ERROR_CNT_A	Bits 13:16 of timestamp error counter

0x0720	R	TIMESTAMP_ERROR_CNT_B	Bits 15:0 of timestamp error counter
0x0722	RW	TTCL_TIME_OFFSET	Master trigger trigger re-issue offset control
0x0724	R	MISSED_TRIG_COUNT	Counter of re-issued trigger messages missed
0x0726	R	DLYD_TRIG_ERR_COUNT	Counter of errors in re-issued triggers
0x0728	RW	PROPAGATION_CONTROL	Controls SerDes command processing
0x07EC	R	FIFO_COUNTER	Number of triggers stored in FIFO
0x07EE	R	TRIG_COUNTER	Number of triggers received
0x07F2	R	USER_COUNTER_0	Number of edges received on NIM input 0
0x07F4	R	USER_COUNTER_1	Number of edges received on NIM input 1
0x07F6	R	USER_COUNTER_2	Number of edges received on NIM input 2
0x07F8	R	USER_COUNTER_3	Number of edges received on NIM input 3
0x07FA	R	USER_COUNTER_4	Number of edges received on NIM input 4
0x07FC	R	USER_COUNTER_5	Number of edges received on NIM input 5
0x07Fe	R	USER_COUNTER_6	Number of edges received on NIM input 6
0x0800	R	USER_COUNTER_7	Number of edges received on NIM input 7
0x0848	RW	sd_config	SerDes configuration register.
0x0860	R	RESERVED	Reserved for future use.
0x0862	R	RESERVED	Reserved for future use.
0x0864	R	RESERVED	Reserved for future use.
0x0866	R	RESERVED	Reserved for future use.
0x0900	RW	fpga_ctrl_reg	Main FPGA Configuration Control Register
0x0902	R	vme_status	Status of VME FPGA
0x0904	R	vme_aux_status	vme aux stat
0x0906	R	spare_registers	spare, unused
0x0908	R	flash_vpen	control VPEN pin of flash memory
0x090A	RW	config_start_low	low half of configuration data start address
0x090C	RW	config_stop_high	high half of configuration data stop address
0x090E	RW	config_stop_low	low half of configuration data stop address
0x0910	RW	config_start_high	high half of configuration data start address
0x0918	RW	vme_sandbox1	for rw testing
0x091A	RW	vme_sandbox2	for rw testing
0x091C	RW	vme_sandbox3	for rw testing
0x091E	RW	vme_sandbox4	for rw testing
0x1000	x	fifo	Allows read/write access to the on board FIFO

Table 1 – Summary list of registers within the MyRIAD

3.3 Register details

Specific bit details of each register are provided in a separate Excel spreadsheet upon request. A few registers are worth pointing out in this higher-level document.

> **Commented [JTA4]:** Must be embedded here or published as separate document. Not halfway.

The Board ID value found at register address 0x0000 is normally 0xE725, where each nibble has a meaning:

- 0xE identifies this board as a MyRIAD.

- 0x7 has to to with identification of the printed circuit board revision

- 0x25 is the major/minor code revision of the firmware.

The HARDWARE_STATUS register at address 0x0020 has many useful stats bits:

- Bit 8 is set if the Digital Clock Manager of the FPGA is locked.

- Bit 10 is set if the SerDes chip is _**not**_ locked to data.

- Bit 11 is set if the reception state machine is locked to data.

- Bit 14 is set if the reception state machine has, at some point, lost lock once achieved. If set this can be cleared by a write to the Pulsed Control Register at address 0x040C.

- Bit 15 is a more stringent version of bit 11.

The Pulsed Control register at address 0x040C provides a number of bits that cause transient reset signals to occur by writing a 1 to the register. The register self-clears upon issuing the resets, so that 1s written to the register clear themselves.

- Bit 0, if set, issues a reset to the SerDes receiver state machine.

- Bit 1 resets the internal timestamp (that counts when no SerDes data is available) to zero.

- Bit 2 resets the 'lost lock' flag (bit 14 of HARDWARE STATUS).

- Bit 3 clears the eight general user counters to zero. The general user counter values increment by one for every pulse received on the corresponding NIM inputs.

- Bit 4 simulates an Imperative Sync command from the master trigger, resetting the timestamp to zero irrespective of whether running locally or from the SerDes.

- Bit 5 resets the board-wide FIFO chips.

Reading the NIM_STATUS register at address 0x0700 provides the value of the eight NIM inputs at the moment of the read.

The board timestamp, a 48-bit value, may be read from addresses 0x070A (bits 47:32), 0x070C (bits 31:16) and 0x070E (bits 15:0).

The control signals of the DS92LV18 SerDes chip are connected to bits of the SD_CONFIG register at address 0x0848:

- Bit 0 drives DEN.

- Bit 1 drives REN.

- Bit 2 drives LINE_LE.

- Bit 3 drives LOCAL_LE.

- Bit 4 drives SYNC.

- Bit 5 drives TPWRDWN.

- Bit 6 drives RPWRDWN.

- Bit 7 sets the 'stringent lock' bit that controls how carefully the SerDes reception state machine checks data from the trigger. If the bit is clear the check is minimal; if the bit is set the check is more stringent (hence the name).

- Bit 15 sets the clock source for the board (0:local oscillator, 1: SerDes).

4   ELECTRICAL & MECHANICAL SPECIFICATIONS

4.1   PC board construction

Standard FR-4, 0.063" thick, gold finish for ease of FPGA assembly.

4.2   Mechanical specifics

6U VME identical to the digitizer and trigger modules of Digital Gammasphere.

4.3   Power and Cooling Requirements

The MyRIAD dissipates less than 10 Watts. VME crates have forced air cooling.

4.4   Front Panel Connector pin-outs

The ECL CTL connector on the front panel is a 10-pin male header with two differential ECL inputs and three differential ECL outputs. The pin-out and orientation is intended to match that of the FERA ADC system cables. The pin polarity and naming convention is shown here. These signals are all available to the firmware for other purposes than FERA.
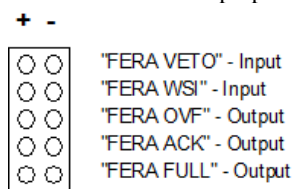
As the MyRIAD firmware currently does not support a FERA interface, the ECL CTL output pins are used to provide some basic diagnostic signals:

- The "FERA FULL" pin pair drives a copy of the multiplexed 50MHz FPGA clock, the output of the clock multiplexer chip.

- The "FERA ACK" pin pair drives a copy of the signal input at NIM input 1. This may be used as a simple level translator.

- The "FERA OVF" pin pair drives a copy of the MyRIAD board's internal 50MHz oscillator. Note that this will be the same as the "FERA FULL" pin signal when the whole board runs from the oscillator, but the two signals will differ when the CLOCK_SEL bit selects the SerDes clock as the multiplex clock.

Similarly, the "FERA WSI" pin pair is used by the current firmware as an alternate source for the "local trigger" signal. The "FERA VETO" input value may be read from a status register for module testing but otherwise has no function.

The ECL I/O connector is similarly polarized with 16 of the 17 pairs used. The bit order is as used for the FERA data connector, shown here. All bits are inputs unless the MyRIAD has been assembled with driver chips.

```
+  -
○ ○    Pin pair is not connected
○ ○    Bit 16
○ ○    Bit 15
○ ○    Bit 14
○ ○    Bit 13
○ ○    Bit 12
○ ○    Bit 11
○ ○    Bit 10
○ ○    Bit  9
○ ○    Bit  8
○ ○    Bit  7
○ ○    Bit  6
○ ○    Bit  5
○ ○    Bit  4
○ ○    Bit  3
○ ○    Bit  2
○ ○    Bit  1
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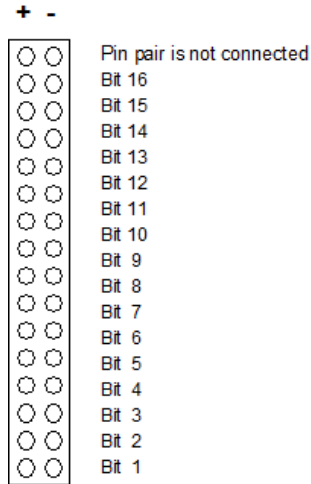
4.5   Front panel LED indicators

A small array of LED indicators provide module status. The LEDs are arranged in a 3x3 array, as shown in Table 2. The numbers indicate which LED, for purposes of description below. The color of the numbered cells is the table indicates the color of the LED when illuminated.

			V
P	1	2	4
F	3	5	6
S	7	8	9

Table 2 – Front Panel LEDs

4.5.1   Indicator Meanings

LEDs #1 and #2 indicate **power** status, as denoted by the silkscreened letter P adjacent to them. Blue LED #1 illuminates if main +5V power is being applied to the board from the VME backplane. Green LED #2 illuminates if the subsidiary voltages developed by the on-board DC-DC converters are present and within tolerance.

LED #4 indicates **VME activity**, as denoted by the silkscreen letter V above it. This LED flashes each time the board is accessed over the VME backplane.

LEDs #3 and #5 indicate **FPGA state**, denoted by the letter F adjacent to them. LED #3 blinks during configuration of the main FPGA. LED #5 is a firmware-specific main FPGA indicator that is, at present, unused.

LEDs #6 through #9 are **general status** indicators, labeled 'S' for "status". These are also controlled by firmware and thus are not fixed in meaning. In the standard Digital Gammasphere and GRETINA builds of MyRIAD firmware, these LEDs are used as follows:

- LED #6 blinks whenever the internal coincidence logic is satisfied.

- LED #7 blinks on leading edges applied to NIM input 1, one of the inputs to the coincidence logic.

- LED #8 blinks on leading edges applied to the local detector TRIGGER IN (firmware selectable between NIM input 0 and the ECL "FERA WSI" input).

- LED #9 blinks on leading edges applied to NIM input 7, a general purpose NIM input.

4.6   NIM inputs and outputs

The MyRIAD provides eight NIM inputs and four NIM outputs at the front panel, arranged as shown in Figure 3. Note that the eight inputs are separated into two groups of four, and that the four outputs are separated into two groups of two, as highlighted by the dashed line boxes in the figure. These dashed lines are not present on the front panel and are included here only for clarity. The letters O and I to the left of each group indicate whether horizontal pairs of connectors are both inputs (I) or outputs (O). The numbers above each connector identify what number input or what number output each connector is.
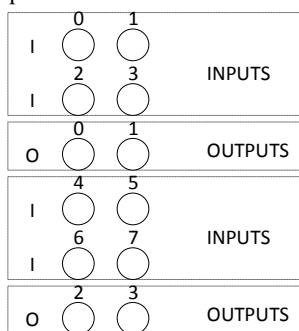
Figure 3 – NIM I/O banks on front panel

The use of NIM inputs 0 and 1 have been previously discussed in this document. The current firmware does not use NIM inputs 2, 3, 4, 5, 6 & 7, leaving them available for future expansion. However, for testing purposes all eight NIM inputs are connected to internal counters that increment on each leading edge applied, so the undefined inputs may be used as general-purpose counters by experiment software.

NIM output 0 is asserted for 20ns when a local trigger has been received.

NIM output 1 is asserted when readout of any of the three timestamp latch registers has occurred, and stays asserted until all three of these registers has concluded. The signal is intended to provide a measurement of the "dead time" during which the lockout logic is active and the timestamp latch cannot be updated.

NIM output 2 is a copy of the 'sync flag' signal sent by the DGS/GRETINA master trigger over the SerDes link and may be used to verify system timing. The 'sync flag' is a pulse that is asserted every 2 microseconds.

NIM output 3 is the coincidence logic output.

5 SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

Proper construction techniques for multilayer circuit boards including solid power and ground planes, sufficient decoupling and fusing were followed in the design of the MyRIAD module. The board is fused at 5Amps on its VCC input.

6 References

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[2] Anderson, J.T.; Brito, R.; Doering, D.; Hayden, T.; Holmes, B.; Joseph, J.; Yaver, H.; Zimmermann, S., **"Data acquisition and trigger system of the Gamma Ray Energy Tracking In-Beam Nuclear Array (GRETINA),"** *Nuclear Science Symposium Conference Record, 2007*. NSS '07. IEEE , vol.3, no., pp.1751,1756, Oct. 26 2007-Nov. 3 2007 doi: 10.1109/NSSMIC.2007.4436499

[3] Simon, M. W.; Gray, R. W.; Cline, D.; Long, C.; Welch, C.; Wu, C. Y., "**CHICO, a compact heavy ion detector for Gammasphere**", *American Physical Society, Division of Nuclear Physics Meeting*, October 2-5, 1996, abstract #AE.01

[4] GRETINA project internal document.

[5]

7   Detailed Register Definitions

The following pages provide detailed descriptions of each register within the MyRIAD firmware. For each register the name and address are provided. A bit-field map is shown detailing which bits are active followed by text describing the function of each bit (or field of bits). Suggestions for typical usage are provided along with the default power-up value of the register. The majority of registers are implemented in the main FPGA firmware, but others associated with firmware maintenance are found in the smaller VME FPGA.

7.1   Main FPGA Registers

The Main FPGA is allocated a subset of the address space by the VME FPGA, of which only a tiny portion is actually used. Control registers are found at addresses 0x0000 through 0x08FC; additionally the main FPGA develops control signals when the FIFO at address 0x1000 is accessed.

7.1.1   *BOARD ID REGISTER – READ ONLY*

Address 0x0000

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Fixed ID value															

7.1.1.1   Value on power-up/reset

0xE725.

7.1.1.2   Function on write

This register is read only. Writes have no effect.

7.1.1.3   Function on read

The register reads a fixed value to identify the board as a MyRIAD and to identify the current firmware revision. The value is somewhat arbitrary, but fixed.

7.1.2 *FIFO STATUS REGISTER – READ ONLY*

Address 0x0004

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	FLAG3	FLAG2	EF_B	PAE_B	HF_B	PAF_B	FFIR_B	DAV	FLAG1	FLAG0	EF_A	PAE_A	HF_A	PAF_A	FFIR_A

7.1.2.1   Value on power-up/reset

0x0000.

7.1.2.2   Function on write

This register is read only. Writes have no effect.

7.1.2.3   Function on read

The register provides status information for the large FIFO that is external to the FPGA of the MyRIAD. The FIFO is implemented as two 16-bit objects, FIFO A and FIFO B, to support either A24/D16 or A32/D32 VME implementations. The current version of firmware is for use in A24/D16 systems and thus only uses FIFO A. The FIFO chip used in the MyRIAD is the SN74V293-10PZA. This FIFO chip has different modes of operation (FirstWordFallThru vs. standard, big endian vs. little endian, etc.). that are selected by various control pin states when the FIFO is reset. The control pins are accessed through the FIFO_CTRL register located at address 0x040E. A careful read of the chip data sheet is strongly recommended to understand all operational modes.

The status bits provided are:

- FLAG0 – FLAG3 are connected to the extra (parity) outputs of the FIFO chips. The corresponding inputs can be driven by the FPGA and may be used as event boundary or other diagnostic bits so that the main FPGA can sense when a particular event is being read out. The current firmware does not utilize this function; it is reserved for future expansion.

- EF_B and EF_A are the **empty** flags of the two FIFO chips, asserted when the chip has no data in it. Depending upon the mode the FIFO is set to, the flag either changes state coincident with the last valid word, or coincident with the first read in which there is no data available to be read (that is, one read later).

- PAE_A and PAE_B are the **partially empty** flags, that assert at a user-defined threshold. Similarly, PAF_A and PAF_B are the programmable **partially full** flags.

- HF_A and HF_B are the **half-full** flags.

- FFIR_A and FFIR_B are dual-purpose status pins that provide either **full flag** or **input ready** status, depending upon how the FIFO has been programmed.

7.1.3 *HARDWARE STATUS REGISTER – READ ONLY*

Address 0x0020

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SD_SM LOCK	1	SYNC	ISYNC	UNQ SM_LK	SD LOCK	X	DCM LOCK		DCM STATUS			CNTR ERR	SD_SM LST_LK	STAT1	STAT0

7.1.3.1   Value on power-up/reset

Depends upon state of board.

7.1.3.2   Function on write

This register is read only. Writes have no effect.

7.1.3.3   Function on read

The register reads back various live status bits that indicate the state of the hardware and firmware. These status bits may be roughly grouped into two sets, SerDes related and non-SerDes. The SerDes status bits are more commonly used:

- The SD LOCK bit is *active low* and reads back the LOCK* signal from the SerDes chip directly. This bit is active (low) if the SerDes chip is able to lock onto some kind of data stream, but does not indicate that the protocol format of the data being received is in any way acceptable. Instead, this is a lower-level physical lock indication.

- The SD_SM LOCK (SerDes State Machine LOCK) bit is set whenever the state machine that monitors data incoming over the 1Gbit SerDes link is, currently, successfully locked onto the expected pattern.

  - The SD_SM_LST_LK (SerDes State Machine Lost Lock) bit is set if any transient loss of lock has been sensed by full-speed logic within the FPGA. Seeing this bit set would indicate that there was either a data transmission error or the clocks were not synchronized. This bit is usually set during initial setup and should be cleared via a write to the PULSED_CTRL register after the link is established. After setup is complete, this bit should be occasionally monitored to catch transient errors. This bit can only be asserted if the SD_LOCK is asserted.

  - The UNQ_SM_LCK (UNQualified State Machine LOCK) is a raw, unfiltered version of SD_SM_LST_LK that is provided only for diagnosis of link issues.

- The SYNC and ISYNC bits are transiently asserted whenever the receiving state machine senses a SYNC command (issued once every 2us) or Imperative SYNC command (issued rarely). These usually change too quickly to be monitored by software.

- The STAT1 and STAT0 bits indicate the state of the two non-SerDes LVDS lines that connect the MyRIAD to the master trigger. At present these are unused and reserved for future expansion.

The non-SerDes status bits are:

- The DCM_LOCK bit is set if the internal Digital Clock Manager logic of the FPGA is locked onto a reference clock. The four-bit DCM_STATUS provides engineering diagnostic codes to indicate what state the DCM control logic is in should the DCM not be working.

- The CNTR_ERR bit is set if the number of events written into the FIFO is different than the number of trigger events counted by the TRIG_COUNTER (number of events captured by the timestamp latch logic). This is an engineering diagnostic bit used only in module firmware testing.

7.1.4 *PULSED CONTROL REGISTER – WRITE ONLY*

Address 0x040C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCM RST	FIFO SD CAPT.	X	TDC RESET	X	X	PH INC	PH DEC	X	X	FIFO RESET	LCL TS RESET	CLR TRIG CNTR	SM LST LK RST	X	X

7.1.4.1   Value on power-up/reset

Always 0x0000.

7.1.4.2   Function on write

The PULSED_CTRL register is used to create various reset/clear/start pulses within the design. Each bit has a uniquely defined function, although multiple bits may be set simultaneously.

- The DCM_RESET bit resets the DCM control logic.

- The FIFO_SD_CAPTURE bit causes the FIFO to capture data as received over the SerDes link, rather than event timestamps, for a programmable number of samples. The number of samples is controlled by the CAPTURE_TIME register.

- The TDC_RESET bit is reserved for future implementation of a time-to-digital converter within the FPGA.

- The PHASE_INC and PHASE_DEC bits cause manual adjustment of the main DCM phase control. Normally the automatic setting is correct, but these may be used to investigate SerDes setup/hold timing.

- The FIFO_RESET bit resets the external FIFO chips.

- The LOCAL_TIMESTAMP_RESET bit resets the timestamp counter to 0, if the MyRIAD is running from its own clock and not receiving the timestamp from a master trigger module.

- The CLEAR_TRIG_COUNTER bit resets the "trigger counter" used by the HARDWARE_STATUS register for FIFO testing.

- The SM_LOST_LOCK_RESET bit resets the SM_LOST_LOCK flag found in the HARDWARE_STATUS register.

7.1.4.3   Function on read

The register self-clears after each write before the VME cycle completes; thus by definition the register always reads back zero.

7.1.5 *FIFO CONTROL REGISTER*

Address 0x040E

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FLAG3	FLAG2	FLAG1	FLAG0	x	x	x	x	x	x	x	x	x	x	BE/LE	FWFT/ SI

7.1.5.1 Value on power-up/reset

Always 0x0000.

7.1.5.2 Function on write

The FIFO CONTROL register is used to set control pins on the FIFO to adjust its operating mode. In the current firmware many of the control pins are fixed to '1' or '0'; the unused bits in this register are reserved for future builds in which additional control pins may be deemed useful.

- The FLAG0 – FLAG3 bits allow the user to set the 'extra', or 'parity', input pins of the FIFO, for testing purposes.

- The BE/LE bit selects whether the FIFO is in Big Endian or Little Endian mode. The new mode does not take effect until the FIFO is reset.

- The FTFT/SI bit sets the general mode of the FIFO. If '0', both FIFOs (A & B) are operated in the "standard" mode. If '1', both FIFOs are in First-Word-Fall-Thru mode. The new mode does not take effect until the FIFO is reset.

7.1.5.3 Function on read

The register reads back whatever was last written to it.

7.1.6 *CAPTURE TIME REGISTER*

Address 0x040E

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Number of samples to capture into FIFO.															

7.1.6.1   Value on power-up/reset

Always 0x0000.

7.1.6.2   Function on write

The CAPTURE_TIME register is used in conjunction with the PULSED_CTRL register to capture SerDes data into the board FIFO for diagnostics. The sixteen bit value in this register defines the number of words to capture in response to the write to the FIFO_SD_CAPTURE bit of the PULSED_CTRL register.

7.1.6.3   Function on read

The register reads back whatever was last written to it.

7.1.7 *CODE REVISION REGISTER – READ ONLY*

Address 0x0600

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PCB revision				Firmware Type				Code Revsion Major				Code Revision Minor			

7.1.7.1   Value on power-up/reset

Fixed constant, dependent upon firmware version.

7.1.7.2   Function on write

This register is read only. Writes have no effect.

7.1.7.3   Function on read

The register reads back as four 4-bit fields. The PCB revision is the physical revision of the board (so far, all boards are 0). The Firmware type is fixed at 0x0B, indicating that this is a MyRIAD. The value for Firmware Type is from a list of module types defined in the Digital Gammasphere experiment. The Code Revision fields (major/minor) indicate the current revision of firmware.

7.1.8 *CODE DATE REGISTERs – READ ONLY*

Address 0x0604 & Address 0x0606

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Two digits for month (e.g. 0x03)								Two digits for day (e.g. 0x31)							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Four digits for year (e.g. 0x2015)															

7.1.8.1   Value on power-up/reset

Fixed constant, dependent upon firmware version.

7.1.8.2   Function on write

This register is read only. Writes have no effect.

7.1.8.3   Function on read

These two registers provide the date of the last firmware revision. The register at address 0x0604 gives the month and day and the register at address 0x0606 gives the four-digit year (e.g. values of 0x0317 and 0x2015 would indicate March 17th, 2015).

7.1.9 *NIM STATUS REGISTER – READ ONLY*

Address 0x0700

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0x00								Logic state of NIM inputs 7:0							

7.1.9.1   Value on power-up/reset

Dependent upon signals applied to front panel.

7.1.9.2   Function on write

This register is read only. Writes have no effect.

7.1.9.3   Function on read

The register provides a snapshot of the logic state of each of the eight NIM inputs as sampled at the moment the register is read. A '1' in any bit indicates that the NIM input is 'active'; that is, current is flowing. Inputs that are pulsing may or may not be captured correctly; there is no edge detection or one-shot logic.

7.1.10 *GATING REGISTER*

Address 0x0702

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TRIG IN SEL	ILA MUX A	FORCE FIFO	ILA MUX B					RESERVED						TS LATCH SOURCE	

7.1.10.1 Value on power-up/reset

Always 0x0001.

7.1.10.2 Function on write

The GATING register provides various selection bits that control when and how the MyRIAD captures timestamps.

- The TRIG_IN_SEL bit selects the input connector used for the "local detector trigger" input. If '0', NIM input 0 is used. If '1', the differential ECL "FERA WSI" pins are used.

- The two ILA MUX bits are used to select what signals are made available to the internal Chipscope internal logic analyzer firmware. Bit 14 selects between two major groups. If bit 14 is '0', then bit 12 provides sub-selection of a subset of the signals between two sources.

- The FORCE FIFO bit, if set, overrides the normal function of the FIFO state machine. In the FORCE FIFO mode, the FIFO captures continuously until the FORCE FIFO bit is cleared, and the FIFO is set to capture SerDes data. This mode is similar to the FIFO_SD_CAPTURE bit in the PULSED_CTRL register but lasts indefinitely as opposed to running for a programmable number of clocks.

- The TS LATCH SOURCE bit pair selects the condition that will cause the timestamp latching function to execute. The two bits provide four possibilities:
    - "00" : no timestamps are latched.
    - "01" : in this state, the default, timestamps are latched whenever the local detector trigger (NIM input 0 or FERA WSI, as selected by the TRIG_IN_SEL bit) is sensed.
    - "10" : timestamps are latched whenever the MyRIAD detects reception of a trigger message from the master trigger over the SerDes link. Note that the timestamp so latched will be the timestamp *of the MyRIAD at the time of reception*, not the timestamp contained within the message from the master trigger.
    - "11" : in this mode, not normally used, timestamps are captured when either the local trigger input occurs or an external trigger message is received.

7.1.10.3 Function on read

The register reads back whatever was last written to it.

7.1.11 *ECL STATUS A REGISTER – READ ONLY*

Address 0x0704

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ECL DATA PORT PIN VALUES															

7.1.11.1   Value on power-up/reset

Depends upon signals applied at front panel.

7.1.11.2   Function on write

This register is read only. Writes have no effect.

7.1.11.3   Function on read

The register reads the logic status of the 16 differential ECL inputs on the front panel data connector.

7.1.12 *ECL STATUS B REGISTER – READ ONLY*

Address 0x0706

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Unused; read 0														WSI	VETO

7.1.12.1   Value on power-up/reset

Depends upon signals applied at front panel.

7.1.12.2   Function on write

This register is read only. Writes have no effect.

7.1.12.3   Function on read

The register reads the logic status of the FERA_WSI and FERA_VETO differential ECL inputs on the front panel data connector.

7.1.13 *LATCHED TIMESTAMP REGISTERS – READ ONLY*

Addresses 0x0708, 0x070A and 0x070C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Address 0x0708: Bits 47:32 of the latched timestamp															
Address 0x070A: Bits 31:16 of the latched timestamp															
Address 0x070C: Bits 15:00 of the latched timestamp															

7.1.13.1   Value on power-up/reset

All three registers read 0x0000 at power up or after a board wide reset.

7.1.13.2   Function on write

This register is read only. Writes have no effect.

7.1.13.3   Function on read

These three registers, taken together, read back the 48-bit timestamp associated with the last local trigger. When the local trigger leading edge is sensed, the full 48-bit timestamp is latched within a single clock cycle. However, since the interface is A24/D16, three VME read cycles are required to read out the latched timestamp. This creates a risk that another local trigger may come in during the time needed to read out the three registers. The MyRIAD addresses this by implementing a two-stage pipeline. A 48-bit register latches the timestamp internally and that 48-bit value is propagated to the register addresses only when they are not being read. A lockout state machine starts when any of the three LATCHED_TIMESTAMP registers is read and stays in place *until all three registers have been read*. During this lockout time, the internal register may be updated by a new local trigger, but the value in the internal register will not be copied to the readable registers here *until the lockout machine is finished.*

Thus, the user is cautioned in two ways:

- These registers may not be polled to determine if a new event has been latched, as such polling will keep the lockout machine always active, blocking the desired information from ever becoming available. If polling is desired, use the FIFO_COUNTER or TRIG_COUNTER instead.
- When an event has occurred and the latch is to be read, always read all three locations.

Due to the inherent risk involved in a 48-bit timestamp being split among three 16-bit registers, use of the board-wide FIFO is recommended for general applications. The FIFO does impose a slightly longer fixed dead time (roughly 100ns, as opposed to ~50ns for the latch), but is simpler to use.

7.1.14 *SERDES COMMAND FORMAT REGISTER*

Address 0x070E

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
COMMAND FORMAT CONTROL VALUE															

7.1.14.1   Value on power-up/reset

0x0000.

7.1.14.2   Function on write

The user may select various operating modes of the SerDes receiver logic using this register. The DGS master trigger, the GRETINA master trigger and the DGS router trigger all have slightly different formats for the trigger command stream. This register allows to user to actively select what format is expected. The values currently supported are

- 0x0000 : DGS master trigger format (default)

- 0x0001 : DGS router trigger format

- 0x0010 : GRETINA master trigger format

The functionality of this register is intimately connected with bit 7 of the SERDES CONFIG register at address 0x0848. Bit 7 of that register is the STRINGENT_LOCK bit. If the STRINGENT_LOCK bit is not set, then basic operation of the MyRIAD (timestamp latching) will work with either the DGS or GRETINA master trigger, irrespective of the value in this SERDES COMMAND FORMAT register. Other frames within the command format do differ between DGS and GRETINA; the user is referred to the *Trigger Timing and Control Link Specification* document[4] for further details.

If the STRINGENT_LOCK bit has been set in the SERDES CONFIG register, the MyRIAD implements additional checks against the data patterns in some of the 20 frames of the command format, and thus the value of this register must be set to match the format of the master trigger driving the MyRIAD or the SerDes reception state machine will lose lock and count errors.

7.1.14.3   Function on read

The register reads back what was last written to it.

7.1.15 *AUX DETECTOR TRIG DELAY REGISTER*

Address 0x0710

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Coincidence process delay count (10ns/count)														

7.1.15.1   Value on power-up/reset

0x0000.

7.1.15.2   Function on write

The AUX DETECTOR TRIG DELAY register is used in the MyRIAD's coincidence logic block. When the latching of the timestamp occurs (as selected by the GATING register), a separate state machine begins a delay count. If NIM input 1 receives a leading edge before the delay count becomes equal to the value in this register, a coincidence is registered. This coincidence causes a message to be sent via the SerDes to the master trigger and may be used to form additional triggers. Additionally, the coincidence will blink a front panel LED.

7.1.15.3   Function on read

The register reads back the last value written to it.