MyRIAD Module Specification

-- PRELIMINARY --

April 23, 2014

Version 1.0

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1. GENERAL INFORMATION

The MyRIAD (Multipurpose gamma Ray Interface to Auxiliary Detectors) module is intended to provide an interface to allow other detector systems that work in concert with Digital Gammasphere to receive the timestamp and triggering information from Digital Gammasphere and use that for synchronization.

1.1. Description of Component & How It Fits Into the System

A MyRIAD sits in the VME crate used for data acquisition in an experiment external to Digital Gammasphere(DGS) or Gretina. A CAT5 cable or optical fiber runs from the master trigger module to the MyRIAD providing bi-directional data communication and clock synchronization between the two systems. External signals from the local detector logic indicative of local triggers are connected to front panel inputs of the MyRIAD. Logic within the MyRIAD latches the master trigger's timestamp when local triggers occur, allowing inclusion of the DGS/Gretina timestamp into the readout of the external detector data stream for later merging of events by timestamp.

The MyRIAD may also function as a gating logic module, receiving trigger messages from master trigger and using those messages to gate local triggers within the external experiment. Similarly, the MyRIAD may simply receive triggers from the external experiment and pass them over the SERDES link so that DGS/Gretina triggering may be gated by the external experiment. The overall connection scheme is shown in Figure 1.

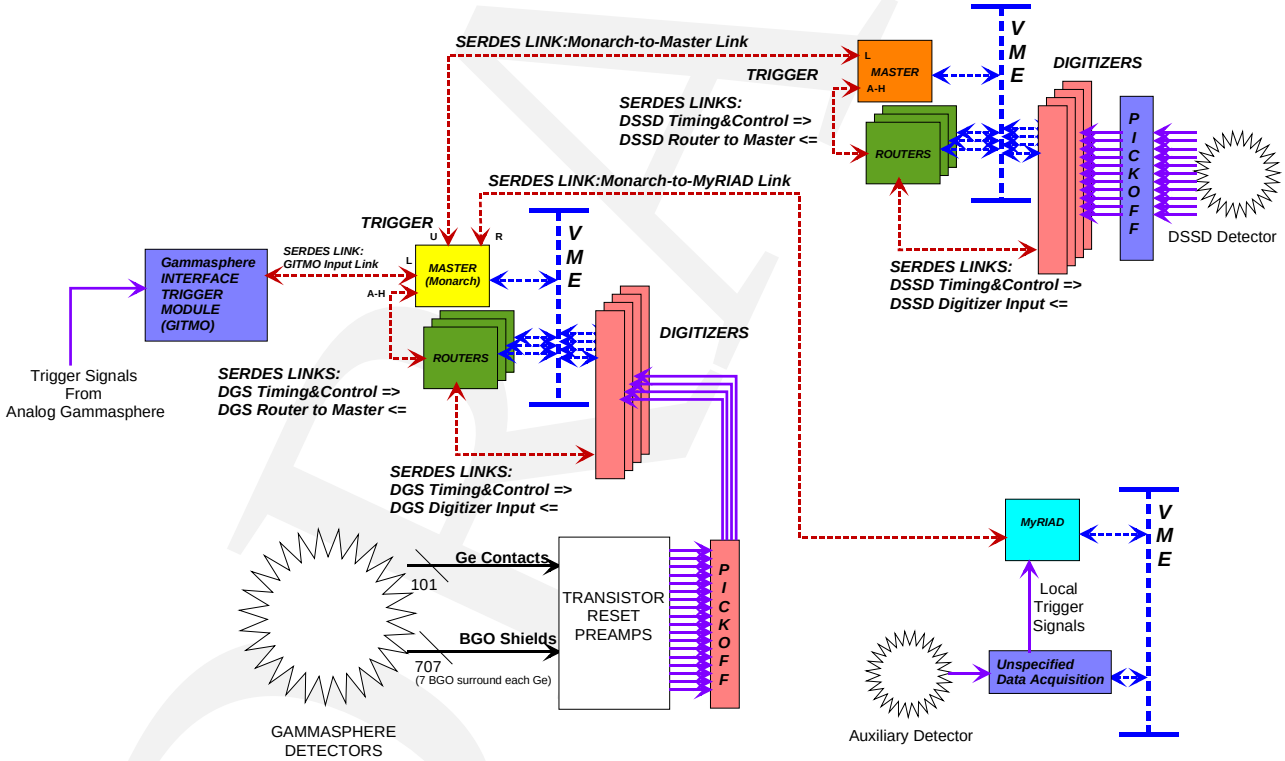


Figure 1 – Overall connectivity between detector systems at Digital Gammasphere

1.2. List of Component Requirements from Specification Hierarchy

The overall requirements of the MyRIAD are as follows:

- SERDES interface compatible with Trigger Timing and Control Link specification (i.e. receive commands like a Router)
- SERDES interface capable of sending triggering information to Master Trigger
- VME 6U module capable of operation in standard or VME64x crate, using either A32/D32 or A24/D16 transaction types
  - Have +3.3V power wiring compatible with either kind of crate – standard VME does not supply +3.3V but VME64x does
  - Have appropriate addressing mechanisms for standard VME (DIPswitch) or VME64x (geographic addressing)
- Provide multiple front panel inputs and outputs in both NIM and differential ECL for interface to a variety of detector logic including other VME modules, NIM and CAMAC
- Provide a registered or buffered mechanism of saving timestamps of events to support either single-event or multi-event data acquisition models in the external detector
- Implement sufficient logic capability to perform windowed timestamp matching and trigger signal gating

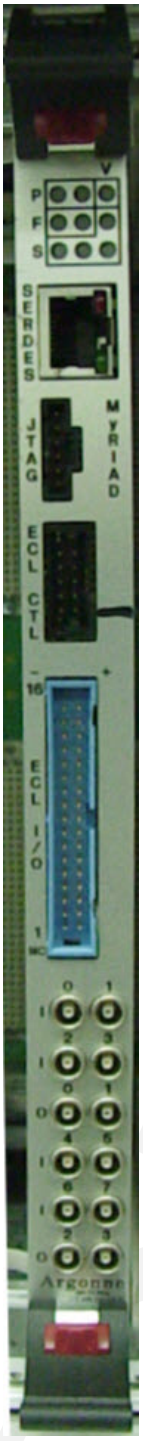
While not a requirement *per se* it is prudent to consider the possibility that some external detector systems may still implement CAMAC ADCs such as the FERA system. 'Analog' Gammasphere provided an interface for such modules to be integrated into the system by use of a custom module that mechanically combined a custom FERA-to-VXI input interface with a commercial (now obsolete and unavailable) VME-to-CAMAC branch highway controller. To accommodate this possibility, the MyRIAD implements sufficient ECL I/O to act as both a FERA readout controller and a FERA input buffer.

1.3. General VME information

The VME mode (A24/D16 or A32/D32) of the MyRIAD is selected by the version of firmware that is loaded into the XC3S400 "VME FPGA" chip. The firmware normally loaded is the A24/D16 version that is compatible with all forms of VME crates. In this version, a DIP switch sets an eight-bit base module address that is compared with bits 23:16 of the VME address asserted by the crate controller. If the upper bits match the MyRIAD will respond to any address within the range 0xdd0000 through 0xddFFFC, where 'dd' is the value set by the DIP switches. Throughout this document reference will be made to register addresses within the MyRIAD. All such addresses shall be described as a four-digit hexadecimal number (i.e. from 0x0000 to 0xFFFC). These addresses should be interpreted by the reader as the lower 16 bits of the 24-bit address range that the MyRIAD has been set to respond to.

The majority of control registers implemented by the firmware in the MyRIAD's FPGAs are readable and writable with the register reading back the last value written to it. All status registers are read-only; writes to status registers have no effect. A few control registers are "write only", used to generate internal timed pulses when 1s are written to certain bits.

1.4. Board Photo - front



Indicator LEDs. The 'V' LED blinks when the board is accessed via VME. The two 'P' LEDs are power status. The two 'F' LEDs indicate FPGA status. The four 'S' LEDs are general status.

The RJ-45 connector is ***NOT ETHERNET.*** This connector uses Cat5e cable for a copper connection to trigger modules only.

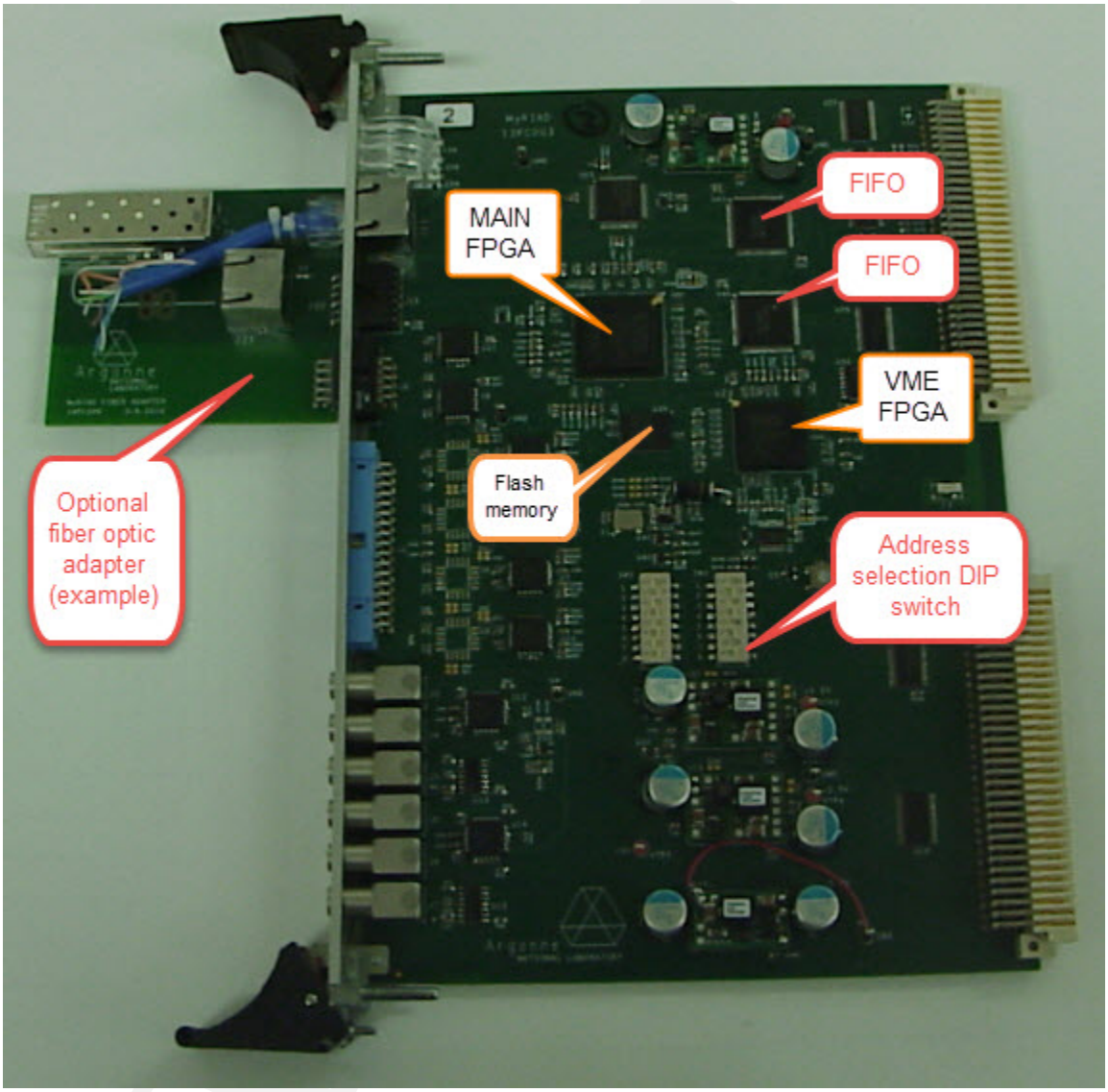
The JTAG connection provides direct access to the FPGAs using a Xilinx JTAG programming adapter.

The ECL CTL connector provides a mix of differential ECL inputs and outputs. The pinout is compatible with the control connector of a FERA interface but the usage of the signals is not fixed; firmware may define them as required.

Similarly the ECL I/O connector provides 16 differential ECL signals for general purpose use. The board provides assembly positions so that either ECL driver chips or ECL receiver chips may be installed. The default is 16 bits of receiver. 100 ohm termination resistors for each differential input are provided.

Eight NIM-level inputs and four NIM-level outputs are provided. Note that the connections are grouped into two sets of four inputs and two sets of two outputs indicated by the letters I (for Input) and O (for output). The usage of all 12 signals is defined by firmware. Normally Input 0 at top left is used as the "local system trigger input".

1.5. Board Photo – side



2. THEORY OF OPERATION AND OPERATING MODES

2.1. Basic Features & Operation (Including Block Diagram)

The MyRIAD is a simplistic device. The VME FPGA handles all the VME cycle decoding and manages firmware download into the Main FPGA. This logic is directly copied from the trigger and digitizer boards. The Main FPGA is a smaller FPGA than in the trigger (Spartan-3 XC3S1000 as opposed to a big Virtex-4 XC4VLX80) to keep costs down. In most cases all the main FPGA has to do is some simple logic and store timestamps. An external large FIFO is provided to handle the possibility of high event rates and/or the FERA readout option as the smaller main FPGA doesn't have much memory.

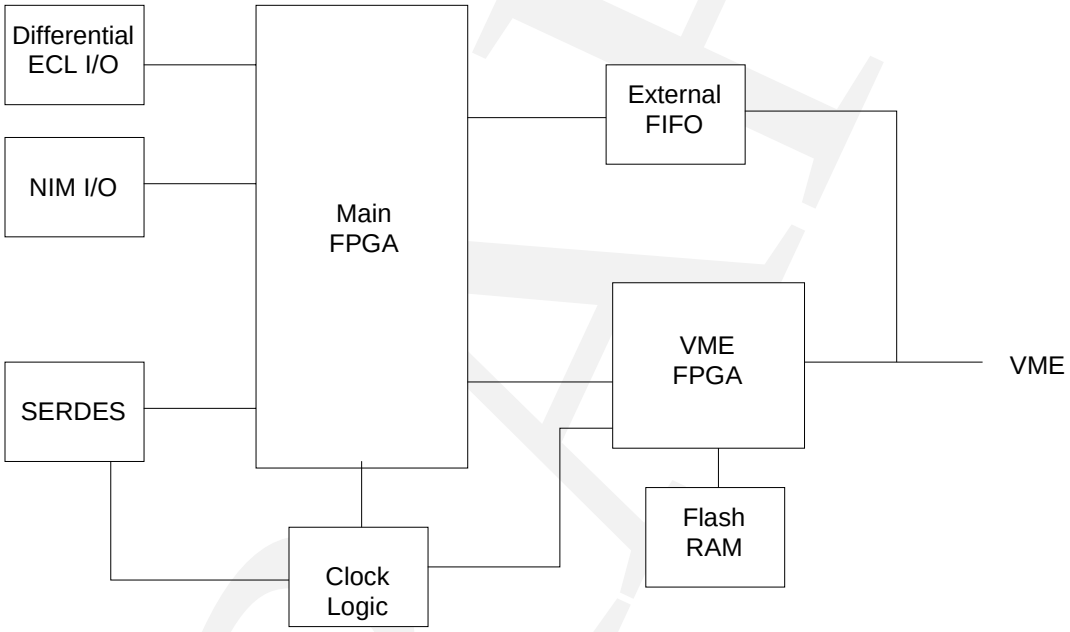


Figure 2 – MyRIAD logic block diagram

2.2. SERDES Data Path

The SERDES data path is bi-directional. Commands, triggers, clock and timestamp are received by the MyRIAD from the Digital Gammasphere Master Trigger. The MyRIAD reports on local trigger conditions read from the NIM and/or ECL inputs back to the Digital Gammasphere Master Trigger over the other half of the SERDES.

2.2.1 Connecting the MyRIAD to the master trigger

The MyRIAD implements a receiver state machine essentially identical to that of the router trigger or the digitizer. User software is required to first note that a physical SERDES link is present by interrogating the SERDES LOCK* signal via bit 10 of the HARDWARE_STATUS register located at address 0x0020. The reception state machine will, immediately upon application of power, attempt to lock onto the command stream from the master trigger but will be unable to achieve lock until the clock of the MyRIAD is phase- and frequency-locked to that of the master trigger. Bit 15 of the SD_CONFIG (SERDES

Configuration) register at address 0x0848 must be set to switch a clock multiplexer chip so that the board runs from the clock extracted from the SERDES data stream before the state machine can reliably lock onto the data of that same stream. The status of the reception state machine may be determined by reading other bits from the HARDWARE_STATUS register.

2.2.2 Trigger communication

The MyRIAD monitors local triggers using a NIM input. A NIM pulse no less than 100ns wide should be used. When the local trigger occurs, a trigger message is sent over the SERDES link from the MyRIAD to the master trigger module containing the timestamp (as latched by the MyRIAD) when the trigger occurred. Control registers within the master trigger then enable or disable re-propagation of the MyRIAD trigger into the master trigger's domain. If enabled, the trigger message from the MyRIAD is retransmitted to all digitizers of the DGS/Gretina system. Any gamma events in the digitizers whose timestamps fit within the time window specified relative to the timestamp in the trigger message are then flagged for readout, allowing the MyRIAD to select gamma events in DGS/Gretina based upon the local trigger of the external detector.

At the same moment that the timestamp of the local trigger is latched by the MyRIAD for transmission to DGS/Gretina, that same timestamp is copied into the board-wide FIFO. If software for the MyRIAD's detector reads out the MyRIAD FIFO as part of every locally triggered event, the DGS/Gretina timestamp is then added to the data for the remote detector allowing software matching of events across detectors by timestamp.

Triggers generated by DGS/Gretina are also received by the MyRIAD over the SERDES link. A NIM output pulses each time a trigger message is received and may be used by local detector logic to form coincidences in the local detector; however this pulse will have significant and variable propagation delay because of the way the DGS/Gretina triggering logic works.

2.3. Control Path Descriptions

As in the trigger boards, the VME FPGA is the overall controller. At power up the VME FPGA loads firmware into the main FPGA from the on-board flash memory and all VME transactions are mediated by the VME FPGA. Reads of the external FIFO over VME are mapped to a specific address by the VME FPGA. All normal control of the MyRIAD is accomplished using register reads and writes over the VME bus.

The MyRIAD receives and processes all command frames from the master trigger module. Future firmware updates will implement support of Auxiliary Detector and Synchronous System Capture commands from the master trigger, allowing the MyRIAD to perform synchronous event rate measurements at the same time such measurements are being made in DGS/Gretina, plus also allow the assertion of control signals to the local detector at specific timestamps for coordination of control actions such as resets, calibration triggers, etc.

3. DETAILED INTERFACE SPECIFICATIONS

3.1. Internal Control Registers

Table 1 shows the list of registers provided within the MyRIAD.

Address	***Register Mode***	***Register Name***	***Function***
0x0000	R	board_id	Contains address and firmware information.
0x0004	RW	FIFO_REG	Contains FIFO status and control
0x0020	R	hardware_status	Contains DCM status information
0x040C	W	pulsed_control	Write only (self clearing) register.
0x0600	R	code_revision	Holds the code revision of the board
0x0604	R	code_date	Reads back code date of compilation
0x0700	R	NIM input status	Reads back current status of NIM inputs
0x0702	RW	gating control	Controls usage of NIM signals to gate triggers
0x0704	R	ECL input status A	Reads back current status of ECL inputs
0x0708	R	ECL input status B	Reads back current status of ECL inputs
0x070A	R	LATCHED_TIMESTAMP_A	Bits 47:32 of latched timestamp
0x070C	R	LATCHED_TIMESTAMP_B	Bits 31:16 of latched timestamp
0x070E	R	LATCHED_TIMESTAMP_C	Bits 15:0 of latched timestamp
0x0710	R	Coincidence window delay	How long to wait after local trigger for match
0x0712	R	coincidence window width	How wide a gate for a GS trig match
0x0800	R	User Counter	Generic user counter, tied to NIM input 7
0x0848	RW	sd_config	SERDES configuration register.
0x0900	RW	fpga_ctrl_reg	Main FPGA Configuration Control Register
0x0902	R	vme_status	Status of VME FPGA
0x0904	R	vme_aux_status	vme aux stat
0x0906	R	spare_registers	spare, unused
0x0908	R	flash_vpen	control VPEN pin of flash memory
0x090A	RW	config_start_low	low half of configuration data start address
0x090C	RW	config_stop_high	high half of configuration data stop address
0x090E	RW	config_stop_low	low half of configuration data stop address
0x0910	RW	config_start_high	high half of configuration data start address
0x0918	RW	vme_sandbox1	for rw testing
0x091A	RW	vme_sandbox2	for rw testing
0x091C	RW	vme_sandbox3	for rw testing
0x091E	RW	vme_sandbox4	for rw testing
0x1000	x	fifo	Allows read/write access to the on board FIFO

3.2. Module Programming

As in the other Digital Gammasphere modules, the program for the VME FPGA is held in a small PROM accessible only by JTAG. The main FPGA program is held in flash memory that is loaded over VME and automatically put into the main FPGA at power-up.

3.3. Register details

Specific bit details of each register are provided in a separate Excel spreadsheet upon request. A few registers are worth pointing out in this higher-level document.

The Board ID value found at register address 0x0000 is normally 0xE725, where each nibble has a meaning:

- 0xE identifies this board as a MyRIAD.
- 0x7 has to to with identification of the printed circuit board revision
- 0x25 is the major/minor code revision of the firmware.

The HARDWARE_STATUS register at address 0x0020 has many useful stats bits:

- Bit 8 is set if the Digital Clock Manager of the FPGA is locked.
- Bit 10 is set if the SERDES chip is ***not*** locked to data.
- Bit 11 is set if the reception state machine is locked to data.
- Bit 14 is set if the reception state machine has, at some point, lost lock once achieved. If set this can be cleared by a write to the Pulsed Control Register at address 0x040C.
- Bit 15 is a more stringent version of bit 11.

The Pulsed Control register at address 0x040C provides a number of bits that cause transient reset signals to occur by writing a 1 to the register. The register self-clears upon issuing the resets, so that 1s written to the register clear themselves.

- Bit 0, if set, issues a reset to the SERDES receiver state machine.
- Bit 1 resets the internal timestamp (that counts when no SERDES data is available) to zero.
- Bit 2 resets the 'lost lock' flag (bit 14 of HARDWARE STATUS).
- Bit 3 clears the general user counter to zero. The general user counter value is read from addrss 0x0800, and the counter increments by one for every pulse received on NIM input 7.
- Bit 4 simulates an Imperative Sync command from the master trigger, resetting the timestamp to zero irrespective of whether running locally or from the SERDES.
- Bit 5 resets the board-wide FIFO chips.

Reading the NIM_STATUS register at address 0x0700 provides the value of the eight NIM inputs at the moment of the read.

The board timestamp, a 48-bit value, may be read from addresses 0x070A (bits 47:32), 0x070C (bits 31:16) and 0x070E (bits 15:0).

The control signals of the DS92LV18 SERDES chip are connected to bits of the SD_CONFIG register at address 0x0848:

- Bit 0 drives DEN.
- Bit 1 drives REN.

- Bit 2 drives LINE_LE.
- Bit 3 drives LOCAL_LE.
- Bit 4 drives SYNC.
- Bit 5 drives TPWRDWN.
- Bit 6 drives RPWRDWN.
- Bit 7 sets the 'stringent lock' bit that controls how carefully the SERDES reception state machine checks data from the trigger. If the bit is clear the check is minimal; if the bit is set the check is more stringent (hence the name).
- Bit 15 sets the clock source for the board (0:local oscillator, 1: SERDES).

3.4. Coincidence Logic within the MyRIAD

A small state machine within the MyRIAD provides some basic coincidence logic for trigger gating. The logic begins operation when the "starting trigger" arrives. Bits 0 and 1 of the GATING_REG register at address 0x0702 select what the "starting trigger" is. When bit 0 is set, the "starting trigger" is the signal applied to NIM input 0 (presumably the local detector trigger). If bit 1 is set, the "starting trigger" is the receipt of a trigger via the SERDES link from the DGS/Gretina master trigger module. Once the "starting trigger" occurs, a delay interval defined by the value in Coincidence Delay Register (address 0x0710) multiplied by 20ns is enforced.

Once the Coincidence Delay time has elapsed, a second timing interval defined by the Coincidence Window Register (address 0x0712) begins. During this second interval, if a signal edge is applied to NIM input 1, a coincidence output signal pulse occurs on NIM output 3. If the second interval elapses without an edge on NIM input 1 the state machine returns to waiting for a "starting trigger".

3.5. Other inputs and outputs

NIM inputs 0, 1 and 7 have been previously discussed in this document. The current firmware does not use NIM inputs 2,3,4,5 & 6, leaving them available for future expansion.

NIM output 0 is an echoed copy of the signal arriving at NIM input 0. Similarly, NIM output 1 buffers a copy of NIM input 1.

NIM output 2 is a copy of the 'sync flag' signal sent by the DGS/Gretina master trigger over the SERDES link and may be used to verify system timing. The 'sync flag' is a pulse that is asserted every 2 microseconds.

NIM output 3, as discussed in section 3.4, is the coincidence logic output.

As the MyRIAD firmware currently does not support a FERA interface, the ECL CTL pins are used to provide some basic diagnostic signals:

- The "FERA FULL" pin pair drives a copy of the multiplexed 50MHz FPGA clock.
- The "FERA ACK" pin pair drives a copy of the signal input at NIM input 1. This may be used as a simple level translator.
- The "FERA OVF" pin pair drives a copy of the MyRIAD board's internal 50MHz oscillator. Note that this will be the same as the "FERA FULL" pin signal when

the whole board runs from the oscillator, but the two signals will differ when the CLOCK_SEL bit selects the SERDES clock as the multiplex clock.

4. ELECTRICAL & MECHANICAL SPECIFICATIONS

4.1. PC board construction

Standard FR-4, 0.063” thick, gold finish for ease of FPGA assembly.

4.2. Mechanical specifics

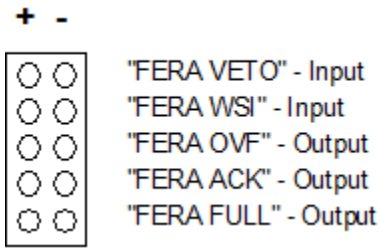
6U VME identical to the digitizer and trigger modules of Digital Gammasphere.

4.3. Power and Cooling Requirements

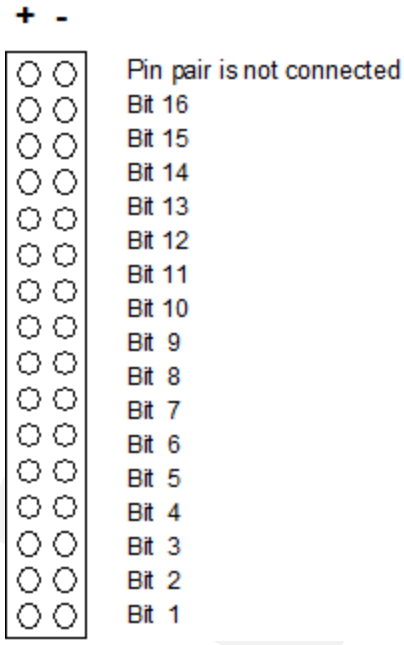
Estimated power dissipation under 10 Watts. VME crates have forced air cooling.

4.4. Front Panel Connector pin-outs

The ECL CTL connector on the front panel is a 10-pin male header with two differential ECL inputs and three differential ECL outputs. The pin-out and orientation is intended to match that of the FERA ADC system cables. The pin polarity and naming convention is shown here.



The ECL I/O connector is similarly polarized with 16 of the 17 pairs used. The bit order is as used for the FERA data connector, shown here. All bits are inputs unless the MyRIAD has been assembled with driver chips.



5. SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

Proper construction techniques for multilayer circuit boards including solid power and ground planes, sufficient decoupling and fusing were followed in the design of the MyRIAD module. The board is fused at 5Amps on its VCC input.