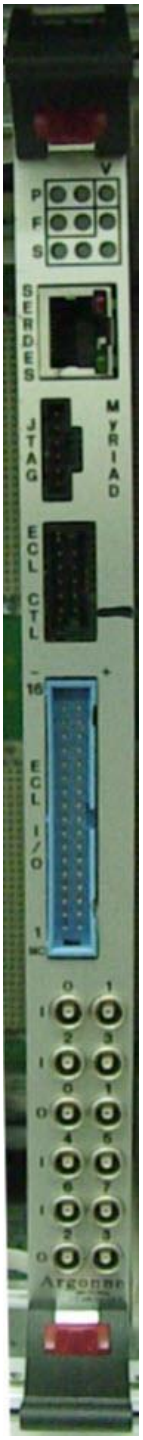
MyRIAD Abridged User Notes

-- I/O CONNECTION REFRESHER --

April 27, 2018
Version 0.0

1 Board Photo - front



Indicator LEDs. The 'V' LED blinks when the board is accessed via VME. The two 'P' LEDs are power status. The two 'F' LEDs indicate FPGA status. The four 'S' LEDs are general status. ***SEE PAGE 2.***

The RJ-45 connector is NOT ETHERNET. This connector uses Cat5e cable for a copper connection to DGS/GRETINA trigger modules only. The LEDs of this connector indicate the state of the connection to the master trigger.

The JTAG connection provides direct access to the FPGAs using a Xilinx JTAG programming adapter.

The ECL CTL connector provides a mix of differential ECL inputs and outputs. The pinout is compatible with the control connector of a FERA interface but the usage of the signals is not fixed; firmware may define them as required. ***SEE PAGE 3.***

Similarly the ECL I/O connector provides 16 differential ECL signals for general purpose use. The board provides assembly positions so that either ECL driver chips or ECL receiver chips may be installed. The default is 16 bits of receiver. 100 ohm termination resistors for each differential input are provided. ***SEE PAGE 4.***

Eight NIM-level inputs and four NIM-level outputs are provided. Note that the connections are grouped into two sets of four inputs and two sets of two outputs indicated by the letters I (for Input) and O (for output). The usage of all 12 signals is defined by firmware. Normally Input 0 at top left is used as the "local system trigger input". ***SEE PAGES 5 & 6.***

2 Front Panel Connector pin-outs

2.1 Front panel LED indicators

A small array of LED indicators provide module status. The LEDs are arranged in a 3x3 array, as shown in Table 2. The numbers indicate which LED, for purposes of description below. The color of the numbered cells is the table indicates the color of the LED when illuminated.

			V
P	1	2	4
F	3	5	6
S	7	8	9

Table 1 – Front Panel LEDs

2.1.1 Indicator Meanings

LEDs #1 and #2 indicate **power** status, as denoted by the silkscreened letter P adjacent to them. Blue LED #1 illuminates if main +5V power is being applied to the board from the VME backplane. Green LED #2 illuminates if the subsidiary voltages developed by the on-board DC-DC converters are present and within tolerance.

LED #4 indicates **VME activity**, as denoted by the silkscreen letter V above it. This LED flashes each time the board is accessed over theVME backplane.

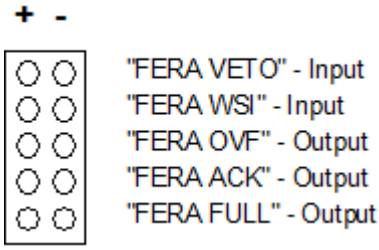
LEDs #3 and #5 indicate **FPGA state**, denoted by the letter F adjacent to them. LED #3 blinks during configuration of the main FPGA. LED #5 is a firmware-specific main FPGA indicator that is, at present, unused.

LEDs #6 through #9 are **general status** indicators, labeled ‘S’ for “status”. These are also controlled by firmware and thus are not fixed in meaning. In the standard Digital Gammasphere and GRETINA builds of MyRIAD firmware, these LEDs are used as follows:

- LED #6 blinks whenever the internal coincidence logic is satisfied.
- LED #7 blinks on leading edges applied to NIM input 1, one of the inputs to the coincidence logic.
- LED #8 blinks on leading edges applied to the local detector TRIGGER IN (firmware selectable between NIM input 0 and the ECL “FERA WSI” input).
- LED #9 blinks on leading edges applied to NIM input 7, a general purpose NIM input.

2.2 ECL CTL Header

The ECL CTL connector on the front panel is a 10-pin male header with two differential ECL inputs and three differential ECL outputs. The pin-out and orientation is intended to match that of the FERA ADC system cables. The pin polarity and naming convention is shown here. These signals are all available to the firmware for other purposes than FERA.



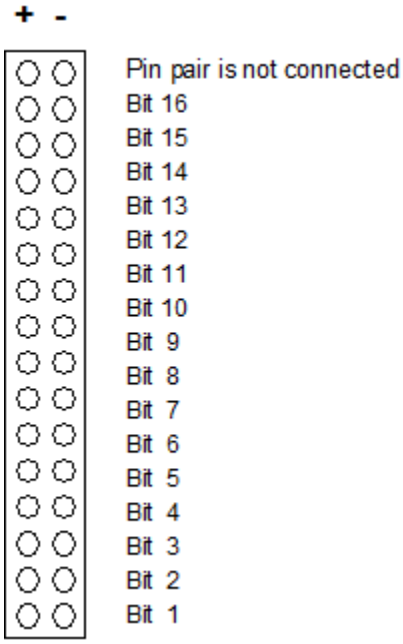
As the MyRIAD firmware currently does not support a FERA interface, the ECL CTL output pins are used to provide some basic diagnostic signals:

- The “FERA FULL” pin pair drives a copy of the multiplexed 50MHz FPGA clock, the output of the clock multiplexer chip. If the MyRIAD is successfully locked to a trigger system over the SERDES this will be the trigger system clock. If not locked, this will be a copy of the MyRIAD’s local oscillator.
- The “FERA ACK” pin pair drives a copy of the signal input at NIM input 1. This may be used as a simple level translator.
- The “FERA OVF” pin pair drives a copy of the MyRIAD board’s internal 50MHz oscillator. Note that this will be the same as the “FERA FULL” pin signal when the whole board runs from the oscillator, but the two signals will differ when the CLOCK_SEL bit selects the SerDes clock as the multiplex clock.

Similarly, the “FERA WSI” pin pair is used by the current firmware as an alternate source for the “local trigger” signal. The “FERA VETO” input value may be read from a status register for module testing but otherwise has no function.

2.3 ECL I/O Header

The ECL I/O connector is similarly polarized with 16 of the 17 pairs used. The bit order is as used for the FERA data connector, shown here. All bits are inputs unless the MyRIAD has been assembled with driver chips.



2.4 NIM Inputs and Outputs

The MyRIAD provides eight NIM inputs and four NIM outputs at the front panel, arranged as shown in Figure 3. Note that the eight inputs are separated into two groups of four, and that the four outputs are separated into two groups of two, as highlighted by the dashed line boxes in the figure. These dashed lines are not present on the front panel and are included here only for clarity. The letters O and I to the left of each group indicate whether horizontal pairs of connectors are both inputs (I) or outputs (O). The numbers above each connector identify what number input or what number output each connector is.

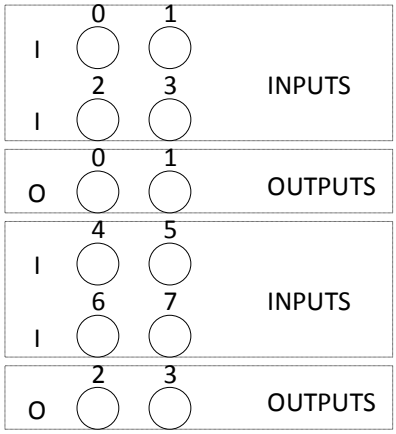


Figure 1 – NIM I/O banks on front panel

2.4.1 NIM Input usage

Every NIM input is connected to a general-purpose 16-bit counter that increments on each leading edge applied. The NIM inputs are sampled at 100MHz and an edge is defined by two adjacent samples having the appropriate (and different) values. The values of all NIM inputs are regularly sampled and sent to the master trigger over the SERDES cable.

NIM input 0 (upper left) is the default connection for the trigger signal from the local detector trigger signal. On each edge of NIM input 0 the timestamp is latched.

NIM input 1 is used for local coincidence logic. When the MyRIAD latches the timestamp (usually in response to an edge on NIM input 0), an internal coincidence timer starts counting. If there is an edge on NIM input 1 before the timeout elapses a local coincidence is asserted. If the timer runs out first a coincidence failure is asserted. The timer value is programmable through a register.

NIM inputs 2 through 7 have no triggering-related function as of April 27, 2018; they are only counted.

2.4.2 NIM output usage

NIM output 0 is multiplexed and can drive one of four signals based upon bits 3:2 of the Gating register (see Section 3):

- SYNC_ERROR_FLAG, asserted if the timestamp from the trigger system is not available;
- AUX_DETECTOR_TRIG, asserted when NIM input 0 has seen an edge;
- SYNC_CAPTURE_FLAG, asserted when a specific command has been received from the trigger over the SERDES link;
- TS_LATCH_BUSY, asserted in response to a trigger and held asserted until the internal logic has finished storing the timestamp in the FIFO.

NIM output 1 is multiplexed and can drive one of eight signals based upon bits 6:4 of the Gating register (see Section 3):

- TTCL_TRIG_FLAG, asserted when a trigger has been sent by the trigger system.
- AUX_DETECTOR_FLAG, asserted when the local detector has indicated a trigger (copy of NIM input 0 or FERA WSI).
- COINC_TRIG_FLAG, asserted when a local coincidence has occurred.
- TS_RELATCH_MON, a diagnostic signal indicative of the board using timestamp *latch* mode as opposed to *FIFO* mode.
- ENCODER_IS_ZERO, a diagnostic signal indicative of a value sent by the trigger system being zero.
- X_MULT_NOT_ZERO, a diagnostic signal indicative of a value sent by the trigger system being non-zero.
- Y_MULT_NOT_ZERO, a diagnostic signal indicative of a value sent by the trigger system being non-zero.
- Eighth option is reserved for future use.

NIM output 2 is a copy of the ‘sync flag’ signal sent by the DGS/GRETINA master trigger over the SerDes link and may be used to verify system timing. The ‘sync flag’ is a pulse that is asserted every 2 microseconds.

NIM output 3 is asserted whenever a trigger accept message has been received from the trigger system, at a programmable delay relative to the timestamp contained within the trigger accept message. This is intended for use with external coincidence or rate monitoring logic, but may also be used to measure the relative delay between the local system trigger and the trigger from the trigger system of the “main” detector.

3 *GATING REGISTER*

The Gating register at address 0x0702 is the most commonly modified register in software as it controls the source of trigger input and the modes of the NIM outputs.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TRIG IN SEL	ILA MUX A	FORCE FIFO	ILA MUX B	RESERVED					NIM OUT 1 MUX CTL			NIM OUT 0 MUX CTL		TS LATCH SOURCE	

3.1 Value on power-up/reset

Always 0x0001.

3.2 Function on write

The GATING register provides various selection bits that control when and how the MyRIAD captures timestamps.

- The TRIG_IN_SEL bit selects the input connector used for the "local detector trigger" input. If '0', NIM input 0 is used. If '1', the differential ECL "FERA WSI" pins are used.
- The two ILA MUX bits are used to select what signals are made available to the internal Chipscope internal logic analyzer firmware. Bit 14 selects between two major groups. If bit 14 is '0', then bit 12 provides sub-selection of a subset of the signals between two sources.
- The FORCE FIFO bit, if set, overrides the normal function of the FIFO state machine. In the FORCE FIFO mode, the FIFO captures continuously until the FORCE FIFO bit is cleared, and the FIFO is set to capture SerDes data. This mode is similar to the FIFO_SD_CAPTURE bit in the PULSED_CTRL register but lasts indefinitely as opposed to running for a programmable number of clocks.
- The TS LATCH SOURCE bit pair selects the condition that will cause the timestamp latching function to execute. The two bits provide four possibilities:
  - "00" : no timestamps are latched.
  - "01" : in this state, the default, timestamps are latched whenever the local detector trigger (NIM input 0 or FERA WSI, as selected by the TRIG_IN_SEL bit) is sensed.
  - "10" : timestamps are latched whenever the MyRIAD detects reception of a trigger message from the master trigger over the SerDes link. Note that the timestamp so latched will be the timestamp *of the MyRIAD at the time of reception*, not the timestamp contained within the message from the master trigger.
  - "11" : in this mode, not normally used, timestamps are captured when either the local trigger input occurs or an external trigger message is received.

3.3 Function on read

The register reads back whatever was last written to it.